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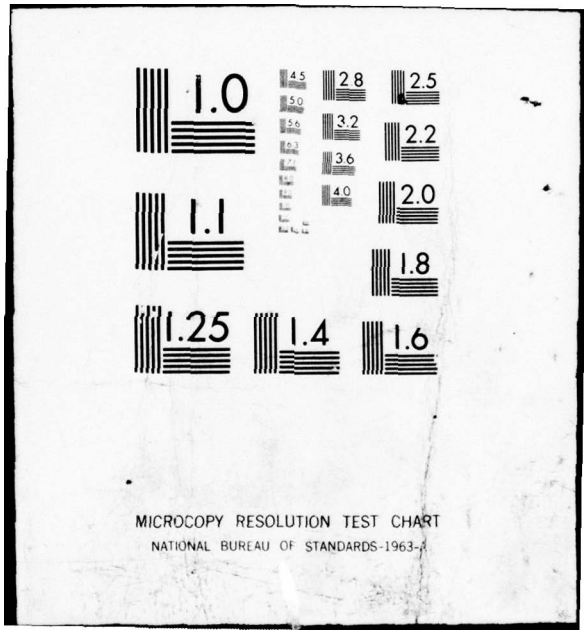
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X-BAND SOLID STATE MODULE

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This interim report covers the second six months of an eighteen-month program to develop an X-band solid state amplifier. The amplifier is the critical component of an all solid state transceiver module for use in active element, airborne, phased array radars. The performance goals are an output power of 5 W with 25 dB gain over the 9 to 10 GHz frequency band with an efficiency (≥) 20% under pulsed conditions.

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Two approaches are being pursued to meet these goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. At the completion of the program, two amplifiers of each type will be delivered.

The effort during this period included continuation of GaAs FET development with emphasis on obtaining devices suitable for the power amplifier stage. The three-stage driver amplifier development was completed. An output power of 1.6 W with 20 dB gain and 26% efficiency over the 9 to 10 GHz frequency band was achieved, meeting the design goals. Extensive pulse measurements have been made on several FET amplifiers, and the results indicate that there are no significant limitations to the use of these amplifiers in active-element, phased-array radar systems.

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PREFACE

This report was prepared by Texas Instruments Incorporated, Dallas, Texas under Navy Contract No. N00173-76-C-0384. The work under this contract is administered and funded by Naval Air Systems Command. Mr. Eliot Cohen of the Naval Research Laboratory, Washington, D. C., is the Scientific Officer.

At Texas Instruments the work is being performed in the Advanced Components Laboratory under the direction of Dr. W. R. Wisseman, Manager of the Advanced Microwave Components branch.

This is the second Semiannual Technical Report for the contract. It covers work done from 1 April 1977 to 30 September 1977. It was submitted by the authors in December 1977.

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SECTION I
INTRODUCTION

This interim report covers the second six months of an eighteen-month program to develop an X-band solid state amplifier. This eighteen-month program is the first phase of a four-phase program that is expected to be completed in a five-year period. The amplifier developed during this phase of the program is the critical component of an all solid state transceiver module for use in active element, airborne, phased array radars. The ultimate goal of the full program is a test bed systems demonstration of a 100-element array.

The amplifier requirements are given in Table 1. Two approaches are being pursued to meet the amplifier performance goals: an all GaAs FET amplifier and an FET/Read diode hybrid amplifier. At the completion of the program, two amplifiers of each type will be delivered.

The GaAs FET fabrication in support of the amplifier development is described in Section II of this report. The device performance and some reliability considerations are also reported. Additional FET and Read diode devices were delivered to NRL during this report period. The microwave performance of these devices is given in Tables A1 through A6 of Appendix A.

Section III details the amplifier development, including the driver amplifier and the output power amplifiers. Specifically, the results of a circuit optimization approach leading to the construction of a driver amplifier that meets the contract goals are described. Results of pulse characterization on single-stage and multistage FET amplifiers are also included in Section III.

Section IV summarizes the progress made during this report period and details plans for the remaining six-month period of this contract.

Table 1

X-Band Solid-State Module

Amplifier Requirements

Center Frequency	9.5 GHz	
1 dB Bandwidth	± 500 MHz	
Peak rf Output	5 W Goal, 4 W Minimum	
Pulse Width	2 - 20 μs	
Duty Cycle	Up to 50%	
Overall Gain	≥ 25 dB	
Final Stage Gain	5 dB Minimum	
Risetime	< 50 ns	
Harmonic and Spurious Output	50 dB Down	
Efficiency	Maximized	
Spectral Purity	at 10 Hz	-48 dB/Hz
	> 1000 Hz	-105 dB/Hz

SECTION II
GaAs FET DEVELOPMENT

A. Device Design and Performance

In the first semiannual technical report for this contract it was reported that the highest output power obtained from a 6400 μm gate width device at 10 GHz with 8 V drain bias was 3.23 W with 4 dB gain. Higher powers could be obtained at higher drain voltages, but the device would be less reliable. During the past six months, this result has not been improved upon significantly, even though a number of slices have been processed and devices tested. This power, though adequate for the power amplifier, is only slightly more than has been obtained from the best 4800 μm gate width devices. The main problem is that the gain is too low. Ideally, about 5 to 6 dB gain is desirable for the power amplifier stage in order to minimize the effect of circuit losses. In addition, two cells (3200 μm gate width) could be used for the third driver amplifier stage if the gain were higher.

The reason for the low gain is twofold: lower than expected single-cell gain and gain degradation when cells are combined. Gate lengths of 1.1 to 1.2 μm have been employed on many slices to increase yield at the gate definition step. Many measurements had shown that devices with such gate lengths have about the same output power with 4 dB gain as those with shorter gates. More recently, when amplifiers were being developed, device gain became more important than maximum output power, and it became apparent that gate lengths of 0.7 to 0.8 μm had 0.5 to 1 dB higher gain. Gate lengths of 0.7 to 0.8 μm are now being employed on all slices, and efforts to increase the yield with this shorter gate length are under way. Another problem is the width of the individual gate fingers. At the beginning of this contract, experiments seemed to indicate that devices with 200 μm fingers would have the same gain as those with 150 μm fingers. However, results from devices fabricated over the past few months indicate that this is not the case; the gain of the 200 μm finger devices may be as much as 0.5 dB less than the 150 μm devices.

This error occurred because the differences being observed are fairly small and of the same order as differences caused by variations in other parameters that occur from run to run.

A more severe cause of gain reduction is the degradation that occurs when multiple cells are interconnected. This happens for both 4800 μm and 6400 μm gate width devices and is typically 1.5 to 2 dB when four cells are interconnected. For example, a single-cell device may have a gain of 9 dB with 9 dBm input power and 5 V drain bias, while a four-cell device with the same drain bias and 15 dBm input power (four times higher) would have only 7 to 7.5 dB gain. This is thought to be largely due to the larger source lead inductance per unit gate width of the multicell device. Source lead inductance acts like a parasitic resistance in series with the device in degrading gain. This problem has been partially solved by bonding wires to ground between each pair of cells. This was accomplished by cleaving single cells from four-cell chips and bonding four of these one-cell chips in parallel, leaving enough space between them for the source bond wires to go to ground. The gain degradation due to interconnection was reduced from 1.7 dB for a four-cell chip of this slice to only 0.7 dB, with about half the loss in the input and half on the output. A 4800 μm gate width device has been designed that accomplishes the same thing during fabrication, and it should be possible to meet the power amplifier requirements with these devices.

To determine the optimum value of I_{dss} for achieving high output powers, the epitaxial thickness was purposely varied across several slices by varying the gate recess depth or taking advantage of an existing thickness variation. The maximum output power with 4 dB gain at 10 GHz is plotted in Figure 1 as a function of I_{dss} for 1200 μm gate width devices from two slices. The drain bias was 8 V in all cases. For both slices the output power rose rapidly with I_{dss} at small I_{dss} and then rose less rapidly when I_{dss} reached 350 to 375 mA.

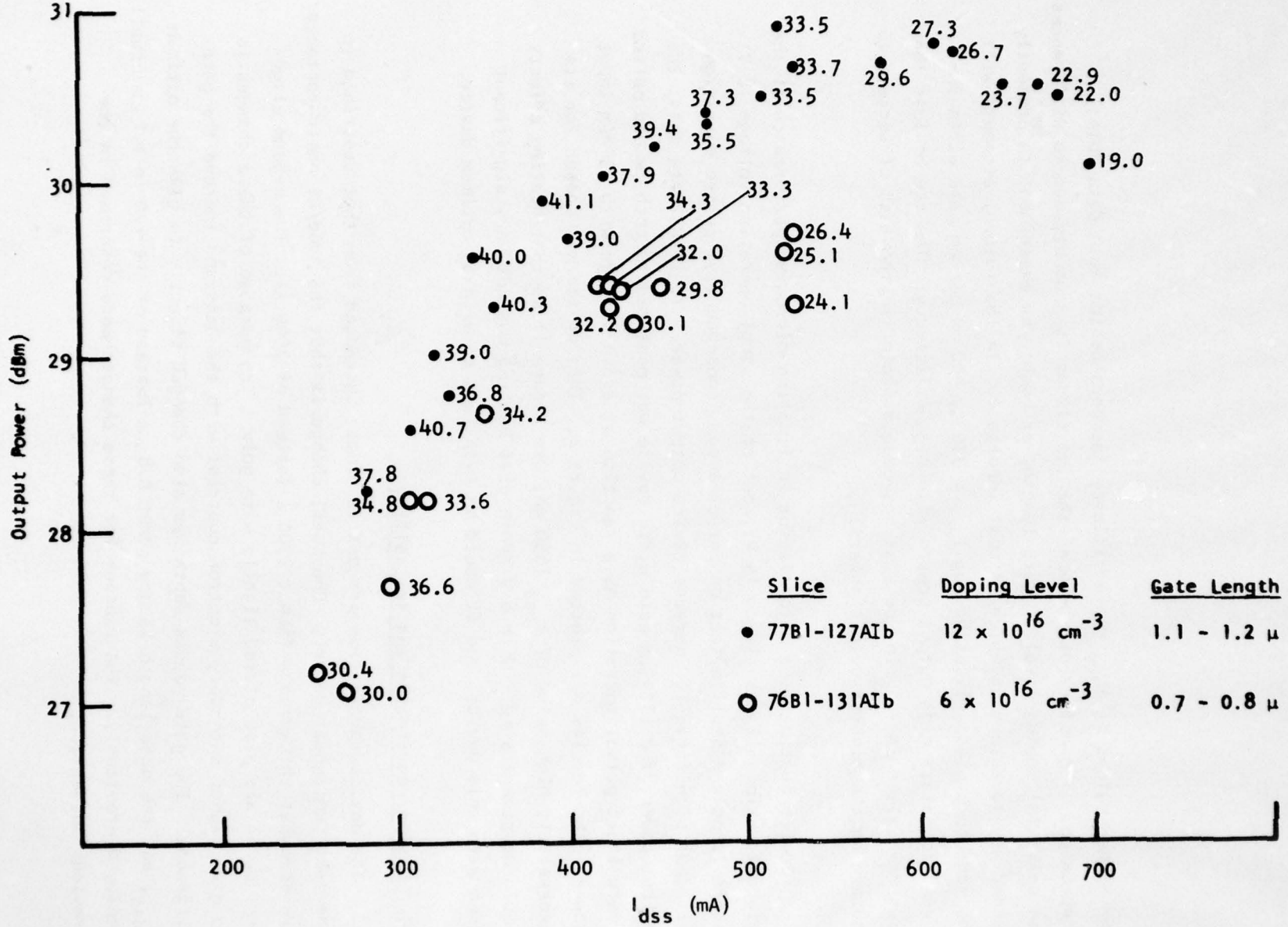

Figure 1 Output Power with 4 dB Gain and 8 V Drain Bias at 10 GHz from 1200 μm Gate Width GaAs FETs as a Function of I_{dss}

At higher values of I_{dss} the efficiency (numbers beside each data point) decreased. The difference between the two slices is probably due to differences in epitaxial doping level or gate length, or both. An experiment is presently under way to determine which is most important. In the future, attempts will be made to process slices having I_{dss} = 330 to 400 mA per mm gate width in order to obtain high output powers with high efficiency. The use of less than optimum values of I_{dss} in the past has been a factor in the lack of success in obtaining the highest output powers.

Device heating is a major factor in limiting microwave performance at the highest drain voltages (12 to 15 V), but at the usual operating voltage (8 V) there is only a small effect on performance. Consequently, pulsed operation will not significantly increase device output power. To illustrate this, the output power of a 1200 μm gate width device was measured in both cw and pulsed (very short pulse) operation as a function of drain voltage with 23 dBm input power. The results are plotted in Figure 2. This device was chosen for its excessively high value of I_{dss} (650 mA; see Figure 1) so that heating effects would be accentuated. With 8 V drain bias heating was not very significant even with this device, and it would be even less so with an optimum device.

B. Device Fabrication and Reliability

The device fabrication process is almost unchanged from that described in the last semiannual report. One small change is that the AuGe/Ni ohmic contacts are somewhat thicker now (about 2700 Å instead of 2000 Å). The e-beam alignment marks are also plated lightly with gold. The purpose of these changes is to give higher secondary electron contrast with the GaAs and improve the gate alignment. The gate recess depth was also changed slightly to give the optimum I_{dss}, and the gate length is now about 0.8 μm instead of the 1.0 to 1.2 μm usually employed previously. The reasons for these changes were described in the previous subsection.

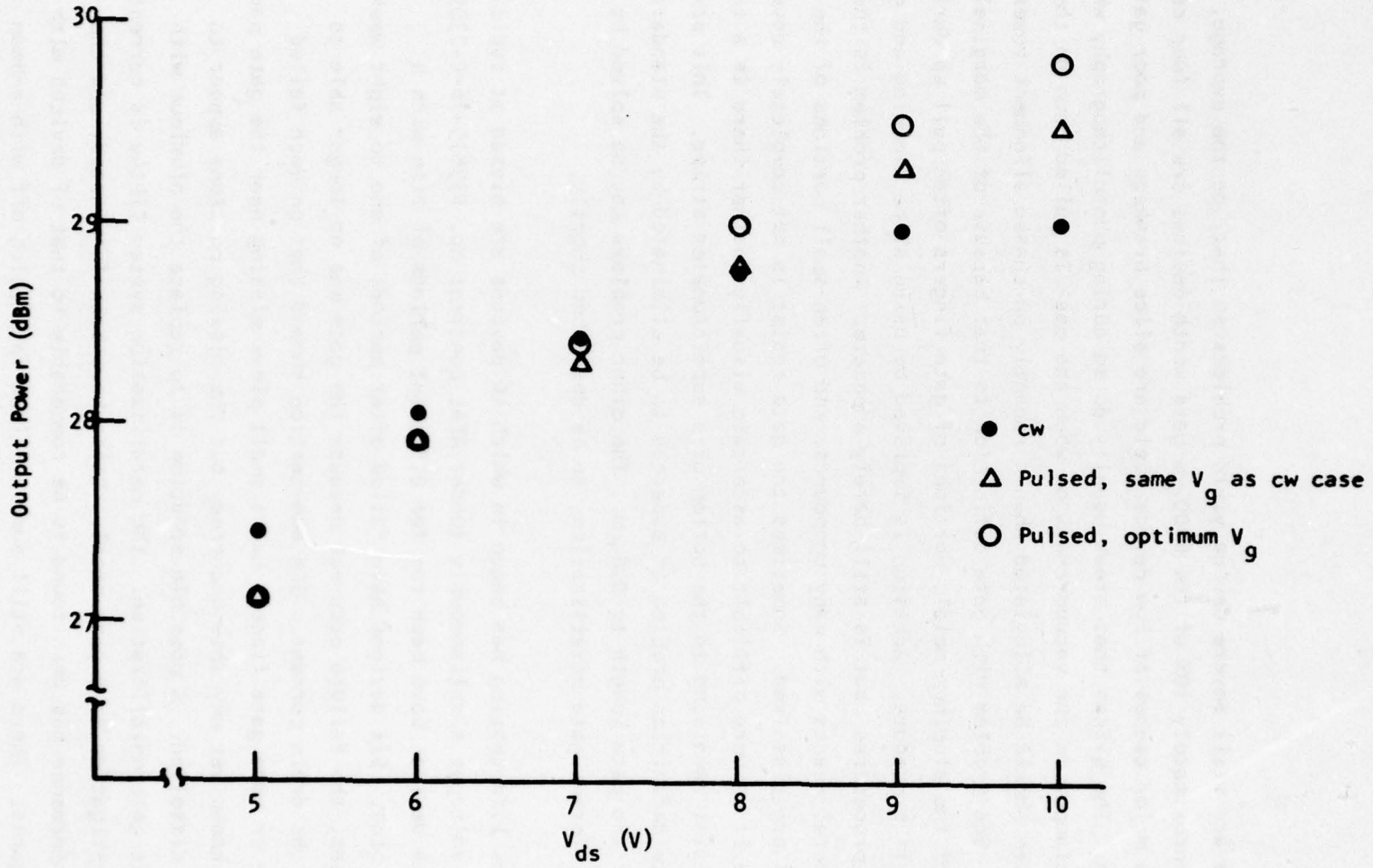

Figure 2 Cw and Pulsed Output Power of a 1200 μm Gate Width GaAs FET as a Function of Drain Bias

There are still severe device yield problems so that, on the average, in only approximately 10% of the 6400 μm gate width devices are all four cells good. The major causes of low device yield are slice breakage and poor gate definition. The slices that break usually do so during photolithography when they are clamped in the vacuum chuck or when the mask is pulled down on them. This problem should be alleviated when a recently purchased alignment tower is received. One problem with gate definition is that because of the marginal adhesion of the aluminum metal, portions of gate fingers often pull up during the lift-off procedure. Adhesion is improved by using slice cleaning and glow discharge procedures, but is still barely adequate. Another problem is that the gate metal reacts with many compounds, and often small portions of the gate metal are dissolved. Sometimes the gate resist is not completely developed out, since it is very difficult to ascertain visually whether there is a thin film of resist remaining in the bottom of a submicrometer stripe. This part of the gate definition problem is expected to be eliminated by the standardization of the gate length to 0.8 μm. The other problems may be solved by using a different gate metallization, to be described shortly.

Device life testing has begun in which 10 devices are biased at typical operating voltages simultaneously (under AFAL Contract No. F33615-76-C-1309). To date, 14 devices have been run for different periods of time with a 50°C heat sink. Six devices have failed after periods of one to eight weeks. In all cases, the failure occurred because the gate was no longer able to pinch off the drain current. SEM examination showed that on each failed device one or more gate fingers had a small piece missing near the gate pad. It is not known yet why this occurred, but the missing portions appear to have been dissolved. A possible solution is to replace the aluminum with a different gate metallization. The metallization system TiPtAu is currently under investigation as a gate metal. Gates have been fabricated, and the device performance has been found to be comparable to that of devices with aluminum gates. There are still some problems in lifting off with e-beam

resist, but these are expected to be solved. The TiPtAu metallization system has several advantages, such as potentially better adhesion to GaAs; much lower susceptibility to attack by processing chemicals or contaminants; lower susceptibility to gate burn-out from high currents or static discharge; compatibility with gold wire bonding; and potential for simultaneous use as a bonding pad metallization, eliminating one mask step.

After several weeks at operating bias, the devices that did not fail exhibited approximately a 5% decrease in I_{dss} and V_p and about 0.2 dB lower small signal gain. First indications are that these changes are greatly reduced with the TiPtAu gates, possibly because the glow discharge process is not used with the TiPtAu metallization.

SECTION III
AMPLIFIER DEVELOPMENT

The circuit work performed during the second six months of this contract included the design and fabrication of the totally integrated FET driver amplifier module and the development of the 5 W output stage. This section of the interim report details the circuit approach used for the development of a compact, totally integrated GaAs FET driver amplifier module[1] and presents data on its microwave performance. Design and fabrication of the high power FET stage using large gate width devices (> 3600 μm) with lumped-element impedance matching are also described. Preliminary microwave performance results of a 5 W FET/Read diode hybrid amplifier are presented. Finally, results of pulse measurements made on both single and multistage FET amplifiers are given.

A. FET Driver Amplifier Development

The solid-state amplifier module (5 W, 25 dB gain over the 9 to 10 GHz band) for the present program is configured to have a GaAs FET driver amplifier to drive either a balanced FET amplifier or a Read diode output stage. The FET driver amplifier is to provide 32 dBm (1.58 W) of output power with 20 dB gain over a 1 dB bandwidth of 1 GHz (9 to 10 GHz). During the first six months of the program, it was demonstrated that a breadboard driver amplifier can be built that can deliver up to 1.58 W output with 19 to 20 dB gain and efficiency approaching 20% across the required bandwidth. Work during the second six-month period has been concentrated primarily on enhancement of the amplifier efficiency and reduction of the amplifier size. For phased-array radar applications, minimization of the size and weight of the individual element is an important design consideration. In addition, the efficiency of each active element must also be maximized. A discussion of technical progress on the GaAs FET driver amplifier follows.

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1. H. Q. Tserng, H. M. Macksey, F. H. Doerbeck, and W. R. Wisseman, "X-Band High-Efficiency MIC GaAs Power FET Amplifier Module," to be presented at 1978 International Solid-State Circuits Conferences, San Francisco, February 1978.

At the beginning of this report period, an improved breadboard driver amplifier was fabricated. Figure 3 shows the gain-frequency response of this three-stage driver amplifier. The drain bias voltage was used as a parameter. It is shown that, at a supply voltage of 9 V, an output power of 1.58 W (32 dBm) with 20 dB gain has been achieved. The overall power-added efficiency of 24% (including bias circuit losses) has also been achieved. The 1 dB bandwidth is 900 MHz (9.1 to 10.0 GHz). The linear gain is 22 dB with the 1 dB gain compression point at 1.36 W output. Except for the narrower bandwidth (0.9 GHz vs the required 1 GHz), the performance of this breadboard amplifier meets the design goals proposed by Texas Instruments. The block diagram of the original driver amplifier design is shown in Figure 4. Figure 5 is a photograph of this breadboard, three-stage amplifier. The individual stages were characterized prior to cascading in the amplifier housing. Discrete resistors and capacitors were used for the dc bias network.

The degree of integration has been further advanced with the design of a compact, three-stage amplifier as shown in Figure 6. The FETs are mounted on small gold-plated copper carriers fitted to slots in the amplifier housing. Input/output and interstage impedance matching are accomplished by the use of a 7.6 mm x 7.6 mm (0.3 inch x 0.3 inch) alumina substrate (0.25 mm thick). The results of the device/circuit optimization during the first six months of the program provided the necessary information on the design of optimum circuit topologies for matching the 300 μm, 900 μm, and 3200 μm gate width FETs used in the first, second, and third stage of the driver amplifier. The amplifier shown in Figure 6 has dimensions of 4.8 cm x 3.3 cm x 1.7 cm (1.9 inch x 1.3 inch x 0.7 inch), excluding input/output SMA connectors.

Several integrated driver amplifier modules were fabricated. Output powers of up to 1.6 W and efficiencies of greater than 20% can generally be obtained within the 9 to 10 GHz frequency band. Figure 7 shows the gain-frequency response of one of the three-stage driver amplifiers. The power

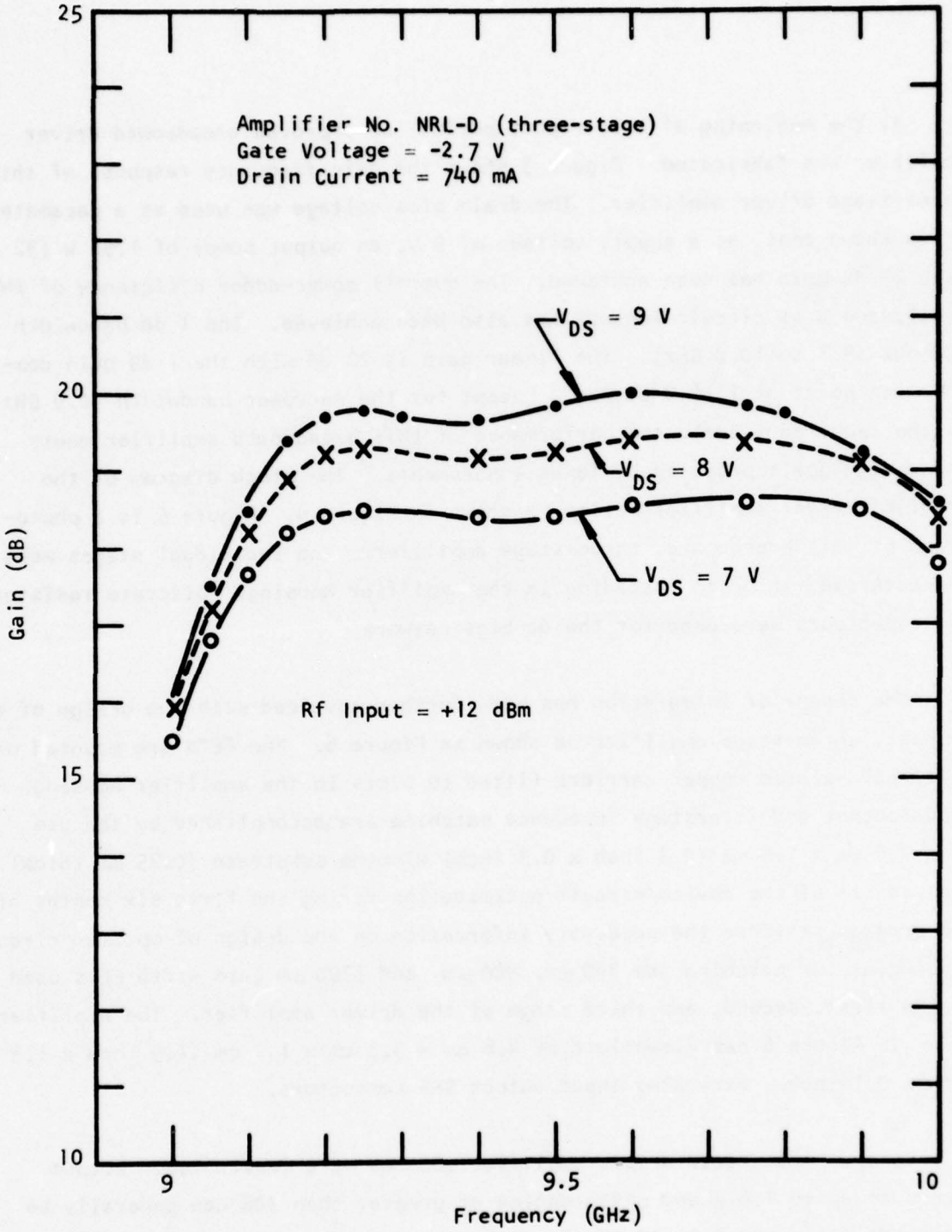
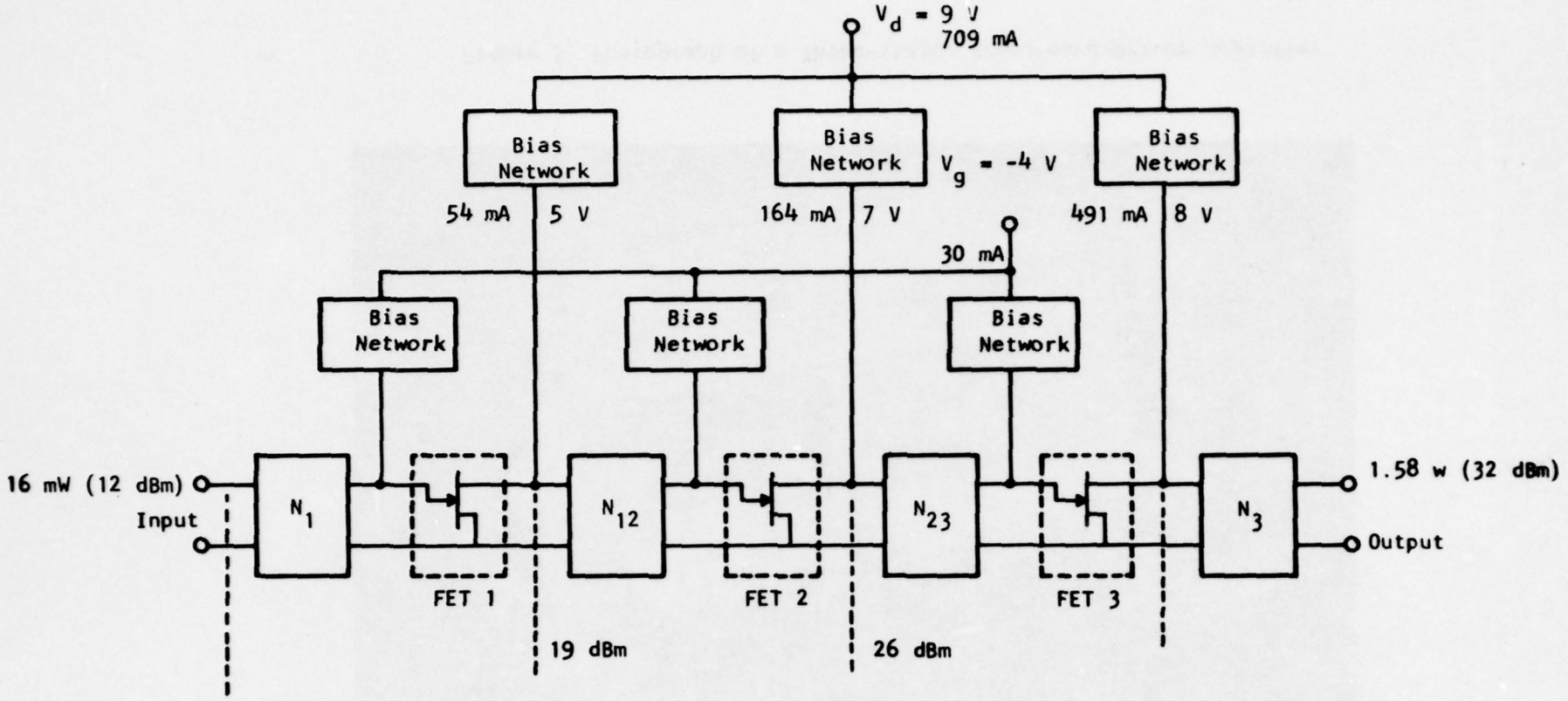


Figure 3 Gain-Frequency Response of a Three-Stage Driver Amplifier



Stage	I	II	III
Gain (dB)	7	7	6
Dc Input (watts)	0.27	1.15	3.93
Rf Output (watts)	0.079	0.400	1.58
Rf Power Added (watts)	0.063	.321	1.18
Power-Added Efficiency (%)	23	28	30

- Total dc Power Input = 6.5 watts
- dc Power Loss in Bias Networks = 1.15 watts
- Amplifier Efficiency Excluding Bias Network Losses = 29.2%
- Overall Amplifier Efficiency = 24%

Figure 4 Block Diagram of a Power FET Driver Amplifier

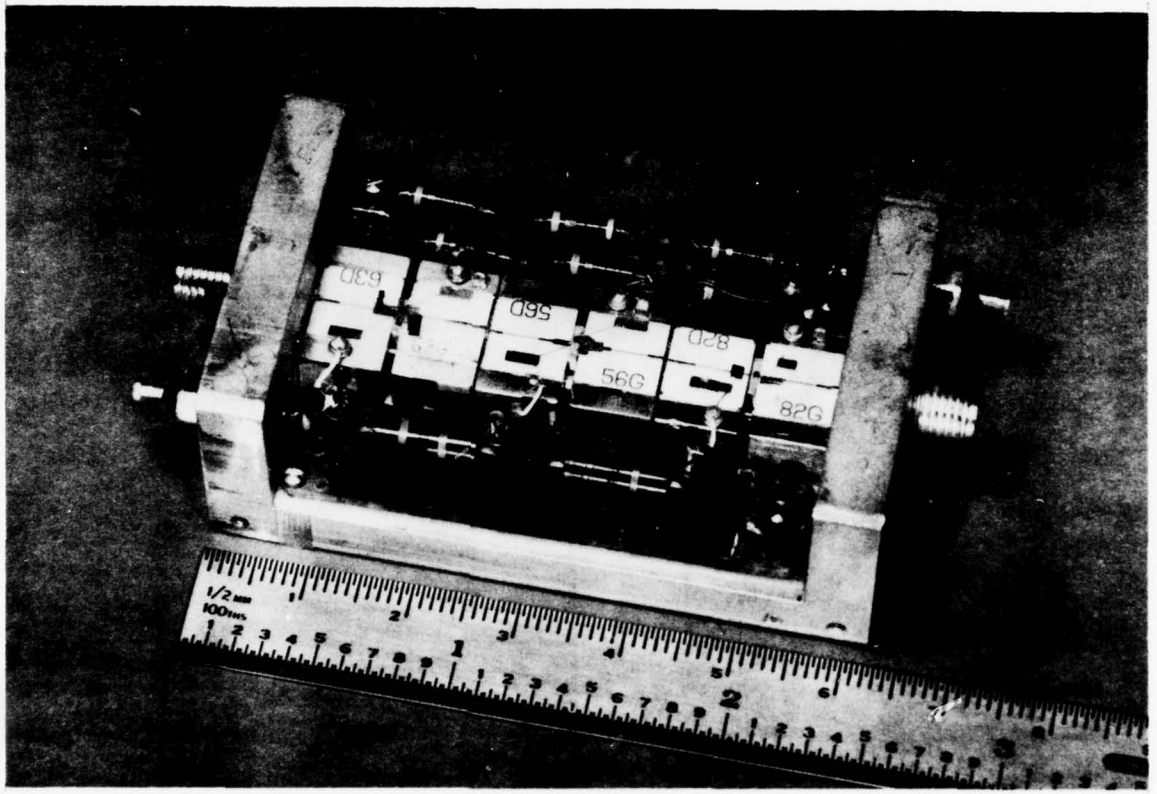


Figure 5 Photograph of a Three-Stage, Breadboard Driver Amplifier

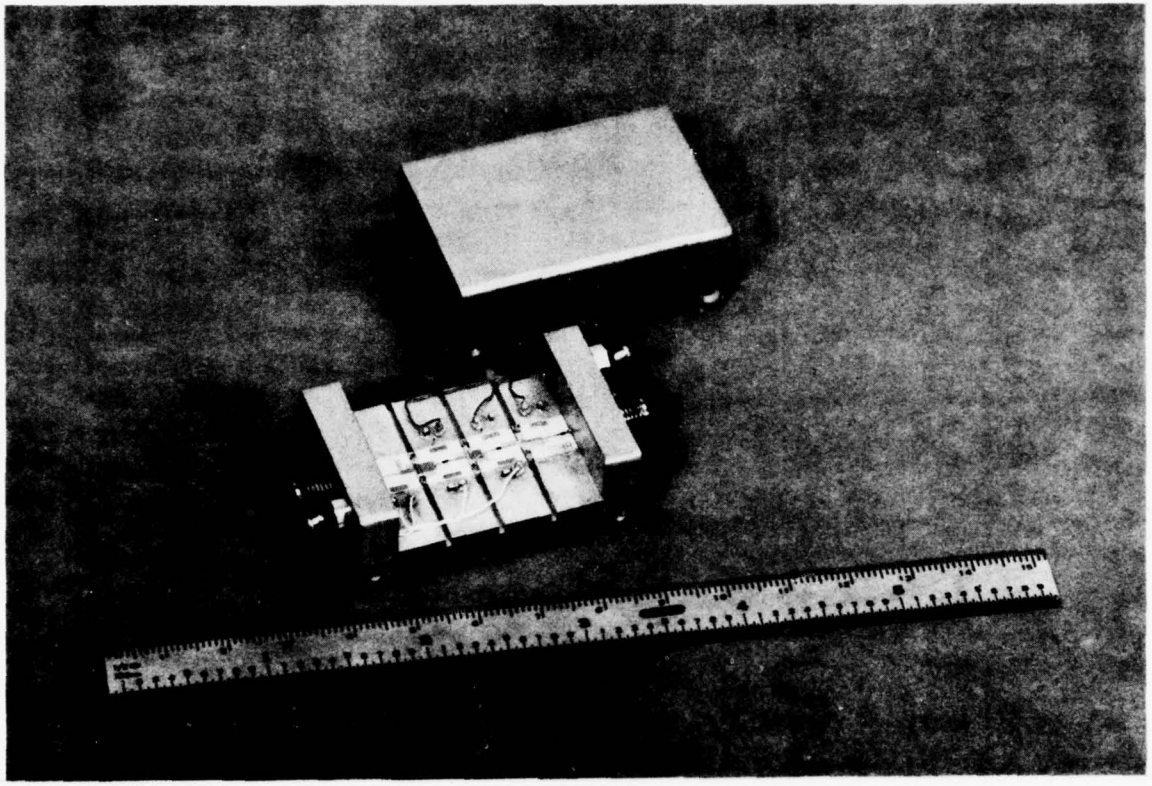


Figure 6 A Totally Integrated, Three-Stage Driver Amplifier Module

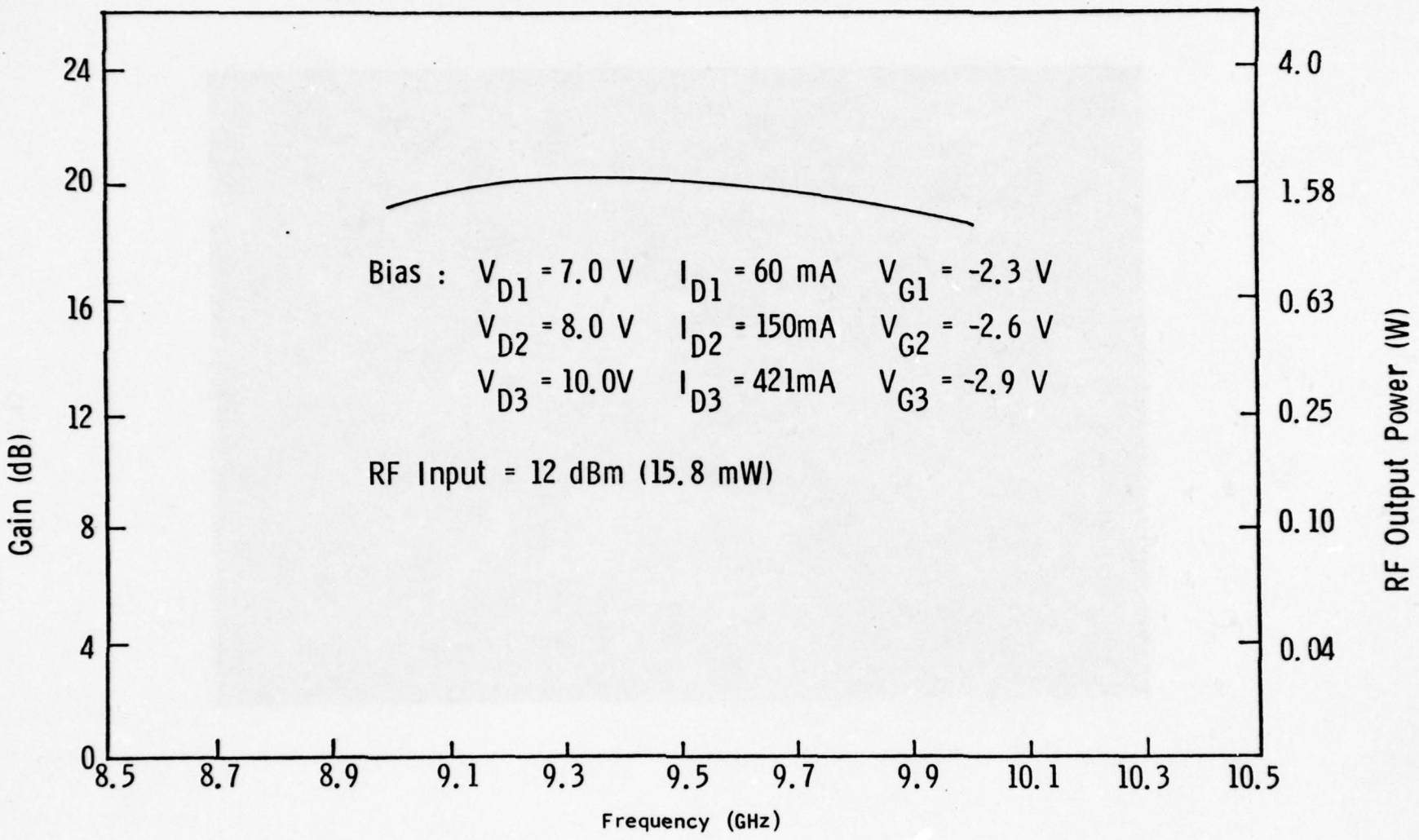


Figure 7 Gain-Frequency Response of a Three-Stage Driver Amplifier With Interstage Matching

supply requirements for the individual stages are also indicated. At 9.5 GHz an output power of 1.66 W with 28% power-added efficiency was achieved. The 1 dB bandwidth is 0.95 GHz (9.0 to 9.95 GHz). Although not shown in Figure 7, the 3 dB bandwidth extends from 7.5 to 10.2 GHz. Figure 8 shows the gain compression characteristic of this amplifier. Linear gain of 25 dB with an output power of $\sim$ 1.2 W can be obtained. The 1 dB gain compression point is 1.4 W. The results shown in Figures 7 and 8 were obtained when the amplifier module was biased with individual power supplies for the different stages. A bias network using chip resistors was subsequently designed and incorporated into the amplifier module. The final module was biased from two power supplies, one for the drains and one for the gates. Because of the bias network losses, the overall power-added efficiency of the module reduces to 26%.

Figure 9 shows the gain-frequency response of yet another driver amplifier module. A 1 dB bandwidth of 1.2 GHz (8.9 to 10.1 GHz) was achieved with 1.58 W (32 dBm) output and 20 dB gain. The power-added efficiency is 24%. It is shown that the design goals as described in Texas Instruments proposal have been met or exceeded in terms of output power, bandwidth, gain, and efficiency.

The wide bandwidth capability of the microstrip matching circuits was demonstrated in an amplifier with the microwave performance shown in Figure 10. One watt of output power was achieved with 18 dB gain at 9.5 GHz with a power-added efficiency of 27%. The 1 dB bandwidth is 2 GHz (8.2 to 10.2 GHz). Figure 11 shows the gain compression curve of this amplifier.

B. FET Output Stage Development

In addition to the fabrication of several integrated driver amplifiers, as discussed above, a considerable amount of circuit effort was devoted to the 5 W FET output stage development. An output power of 5 W with 5 dB gain in a balanced amplifier configuration was used as the circuit approach. Figure 12 shows the circuit layout of the all-FET power amplifier module. The output

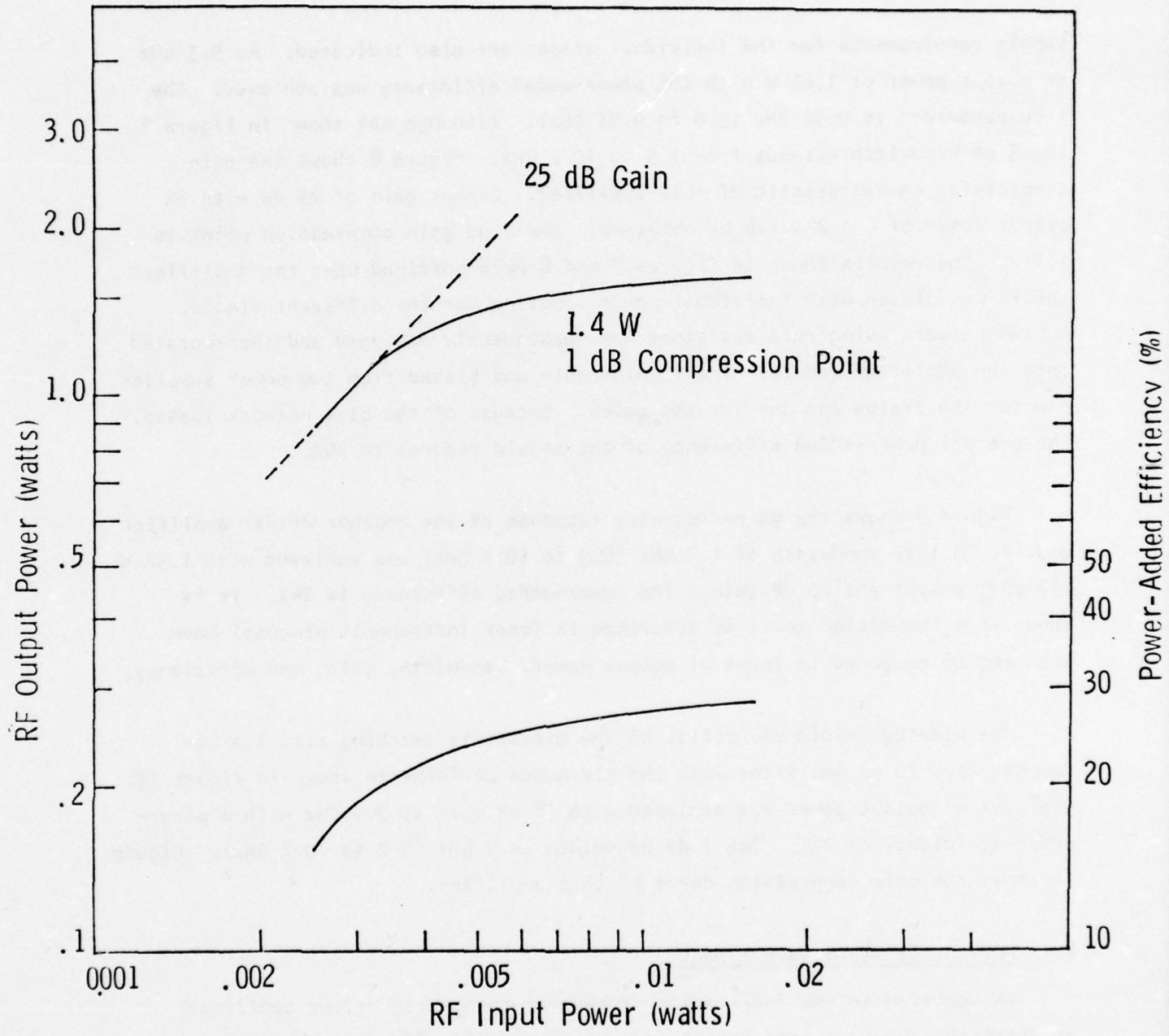


Figure 8 Output Power and Power-Added Efficiency of a Three-Stage Driver Amplifier as a Function of Input Power at 9.5 GHz

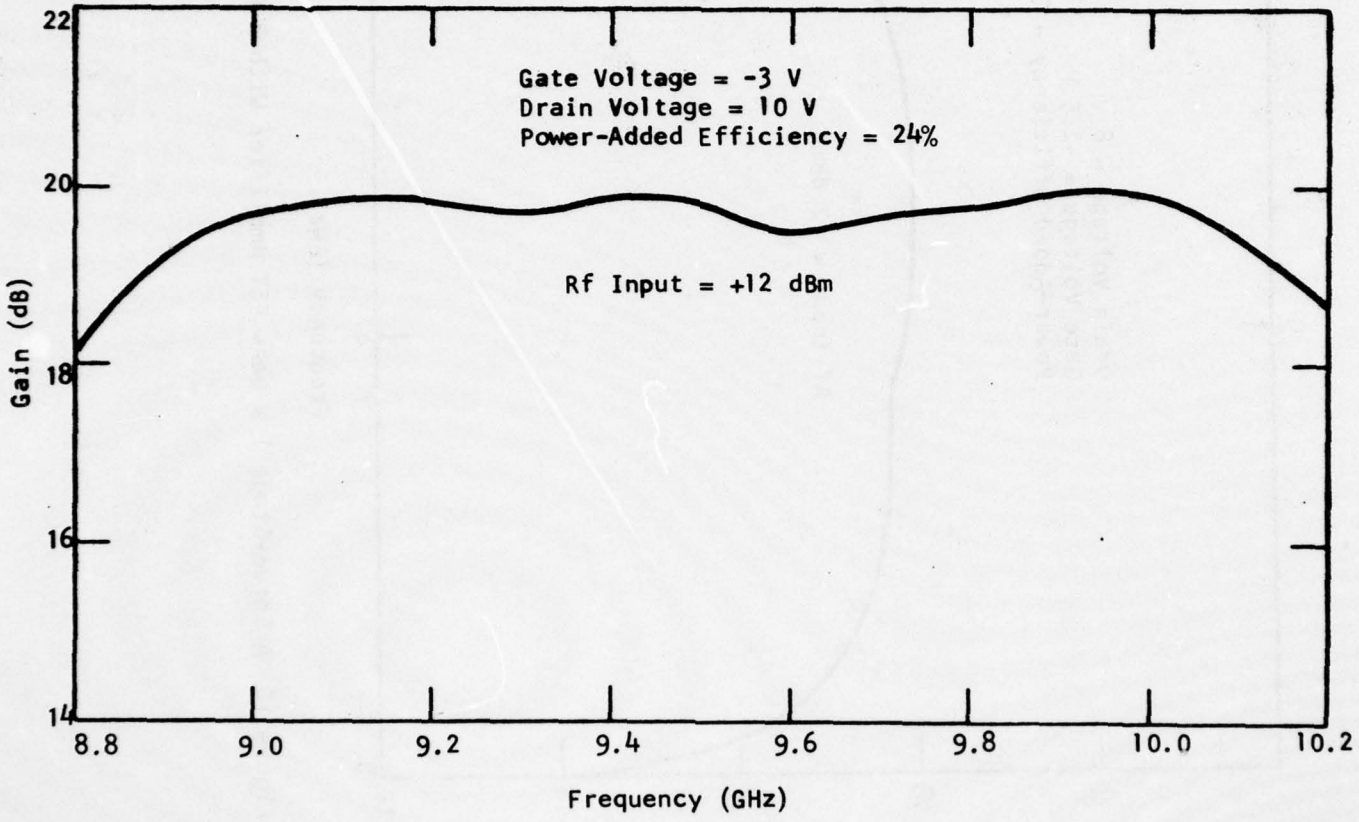


Figure 9 Gain-Frequency Response of a Three-Stage Driver Amplifier

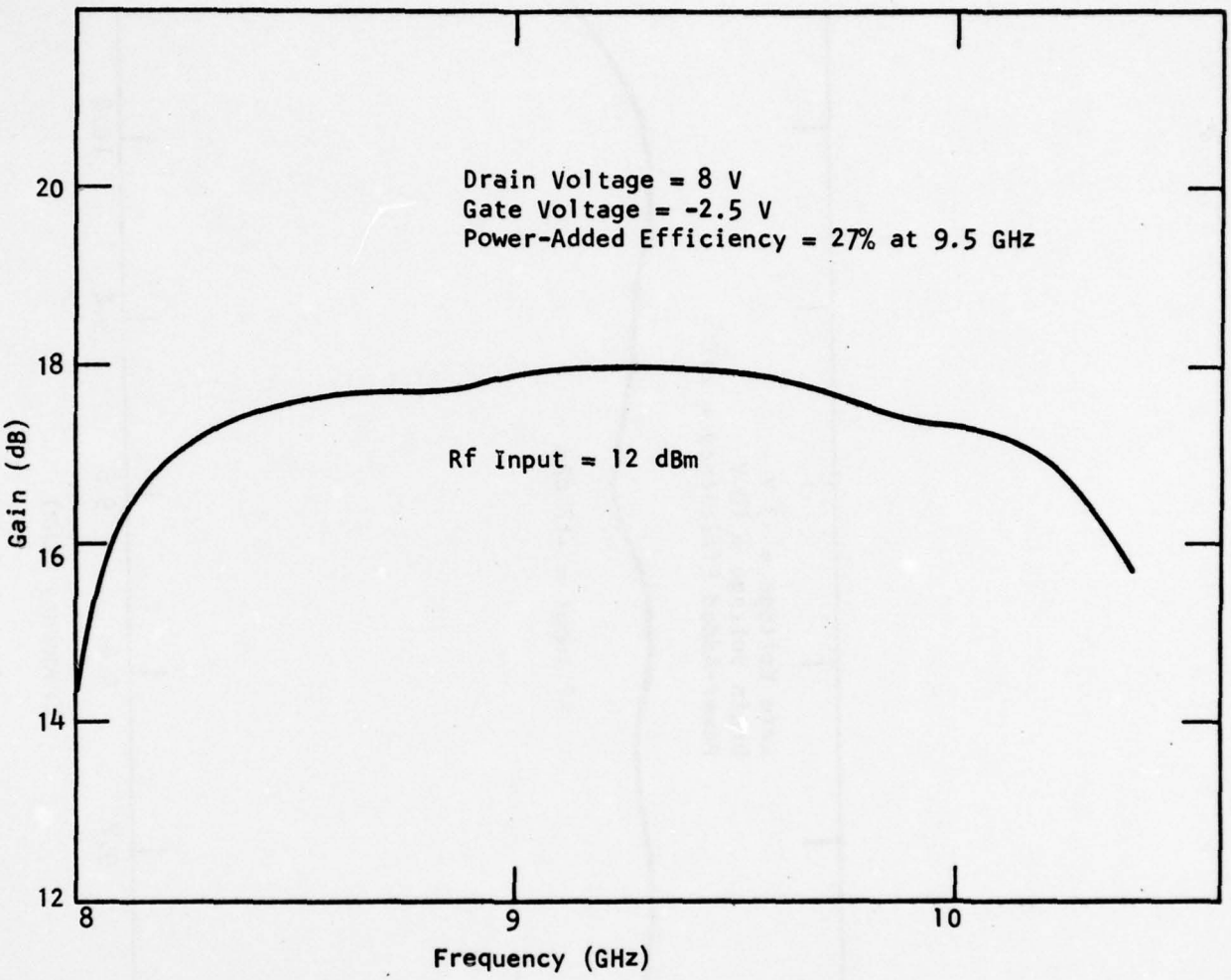


Figure 10 A Three-Stage 1 W GaAs FET Amplifier With 2 GHz Bandwidth

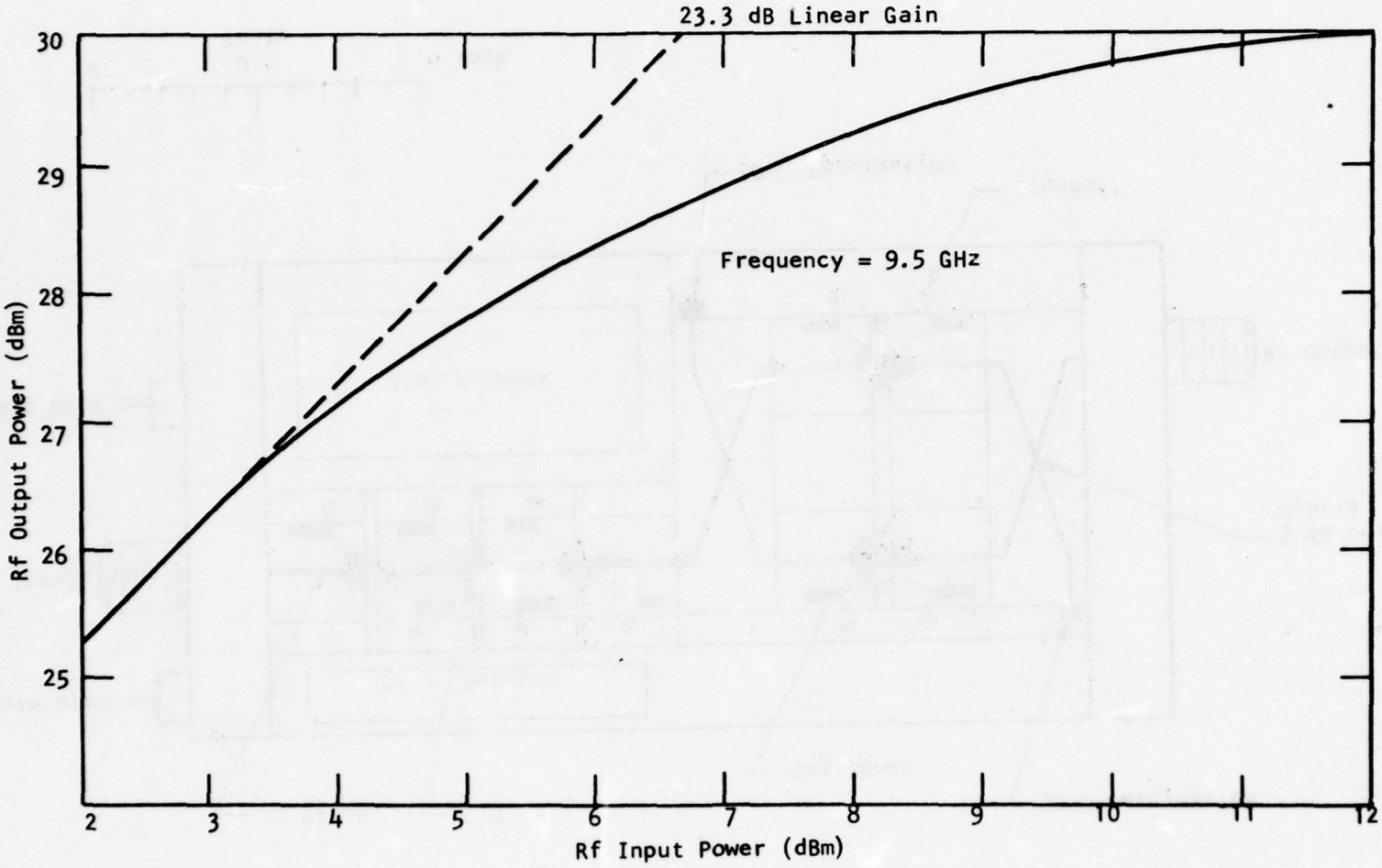


Figure 11 Compression Characteristics of the 1 W Amplifier

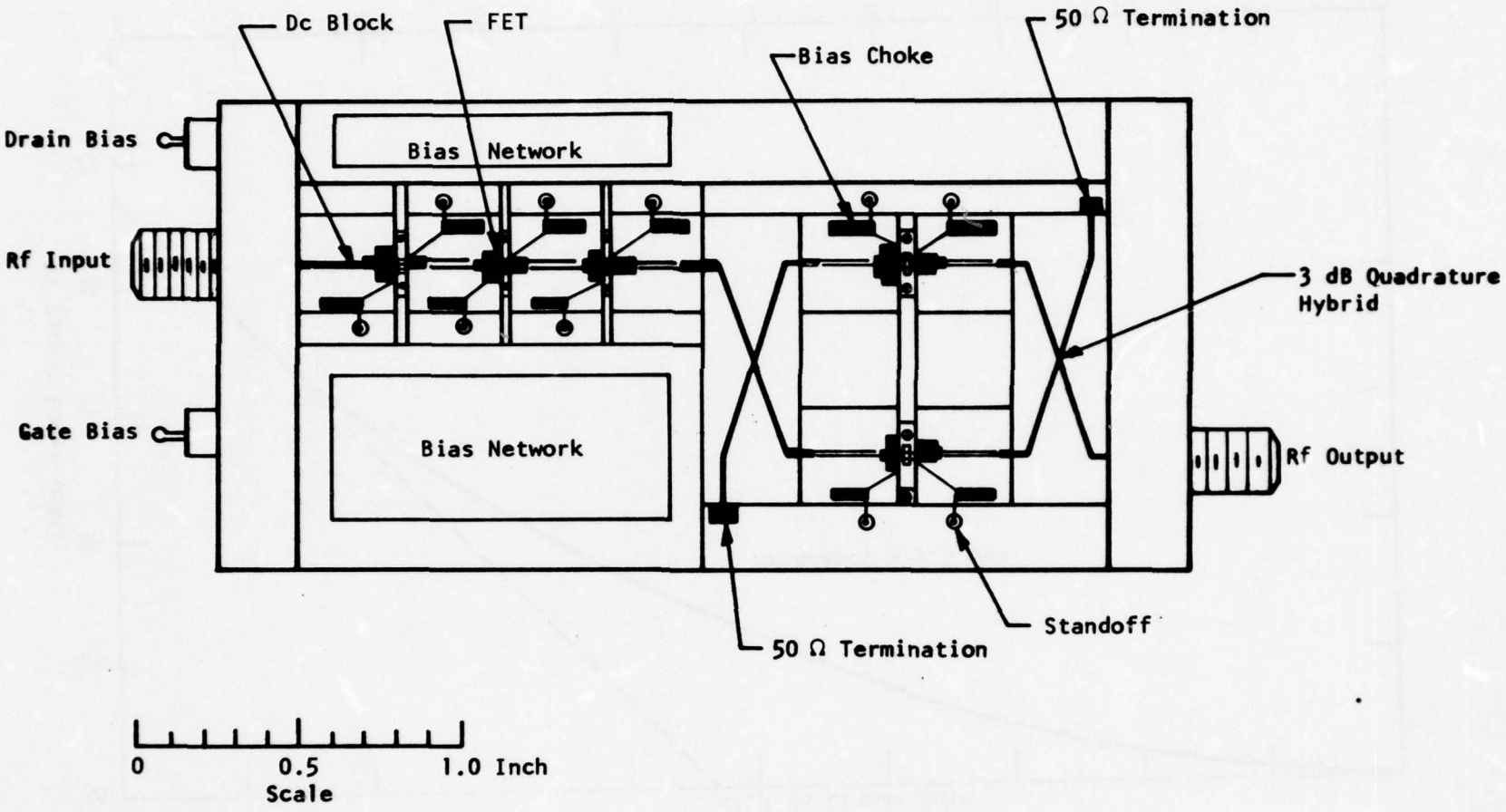


Figure 12 Circuit Layout of the All-FET Power Amplifier Module

stage, consisting of input/output 3 dB hybrid and the two component amplifier matching circuits, will be built on a separate carrier plate for flexibility of characterization prior to module integration. During this report period, the principal circuit emphasis for the high-power output stage development was to devise an optimum circuit for the 6400 μm gate width device. For this purpose, the use of lumped LC elements for "impedance matching on the chip" was extensively pursued. This technique allows for combining more cells at the chip level while still maintaining a manageable impedance level for matching to the 50 Ω source and load.

Figure 13 shows the circuit topology using lumped elements for impedance matching. The values of the input/output shunt capacitances can range from 0.6 to 1.2 pF. The inductances are on the order of 0.3 to 1.5 nH and can be realized with bonding wire inductances. Silicon MOS capacitors were used as the matching elements. Figure 14 shows a photograph of an "internally matched" 6400 μm gate width FET. An output power versus frequency characteristic of a single-stage, four-cell (6400 μm gate width) FET amplifier with internal matching is displayed in Figure 15. At 9.4 GHz, an output power of 3.6 W with 3.6 dB gain was obtained with 18% power-added efficiency. With the availability of additional high gain devices and with further improvement in cell-combining efficiency, output powers of 3 W with 5 to 6 dB gain will be achievable. Attempts will be made to combine two 3 W amplifiers in a balanced configuration to achieve the 5 W output power goals. Figure 16 shows a test fixture for the balanced output stage.

C. FET/Read Hybrid Amplifier Performance

The second amplifier configuration for this program consists of a GaAs FET driver amplifier and a GaAs Read diode amplifier as the output stage. The driver amplifier development was discussed earlier in this report. Preliminary results for a breadboard hybrid FET/Read amplifier were obtained by cascading an FET driver amplifier with a Read diode amplifier. The gain frequency response

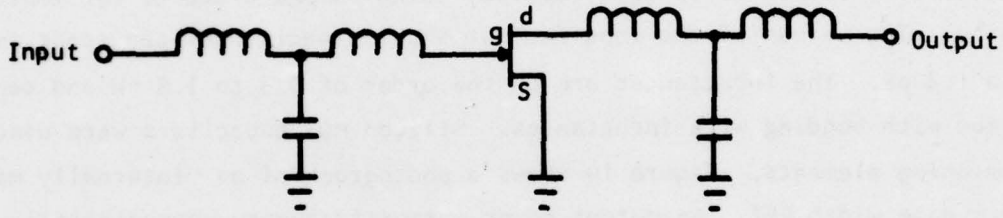


Figure 13 Circuit Topology for Matching GaAs FET With Lumped LC Elements

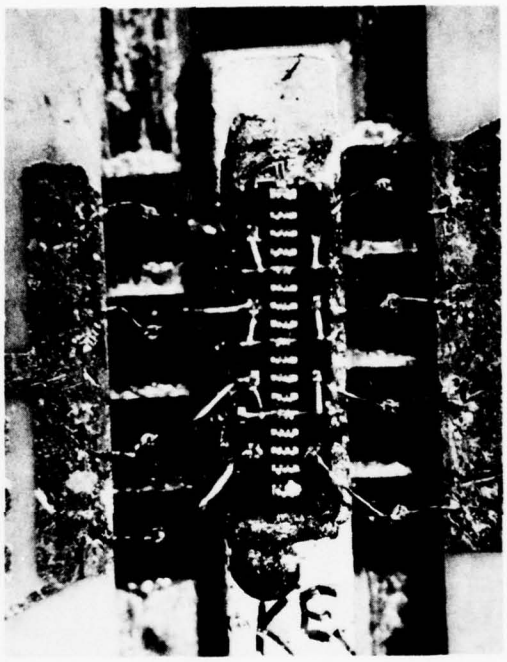


Figure 14 Photograph of a Four-Cell GaAs FET Amplifier With Internal Matching

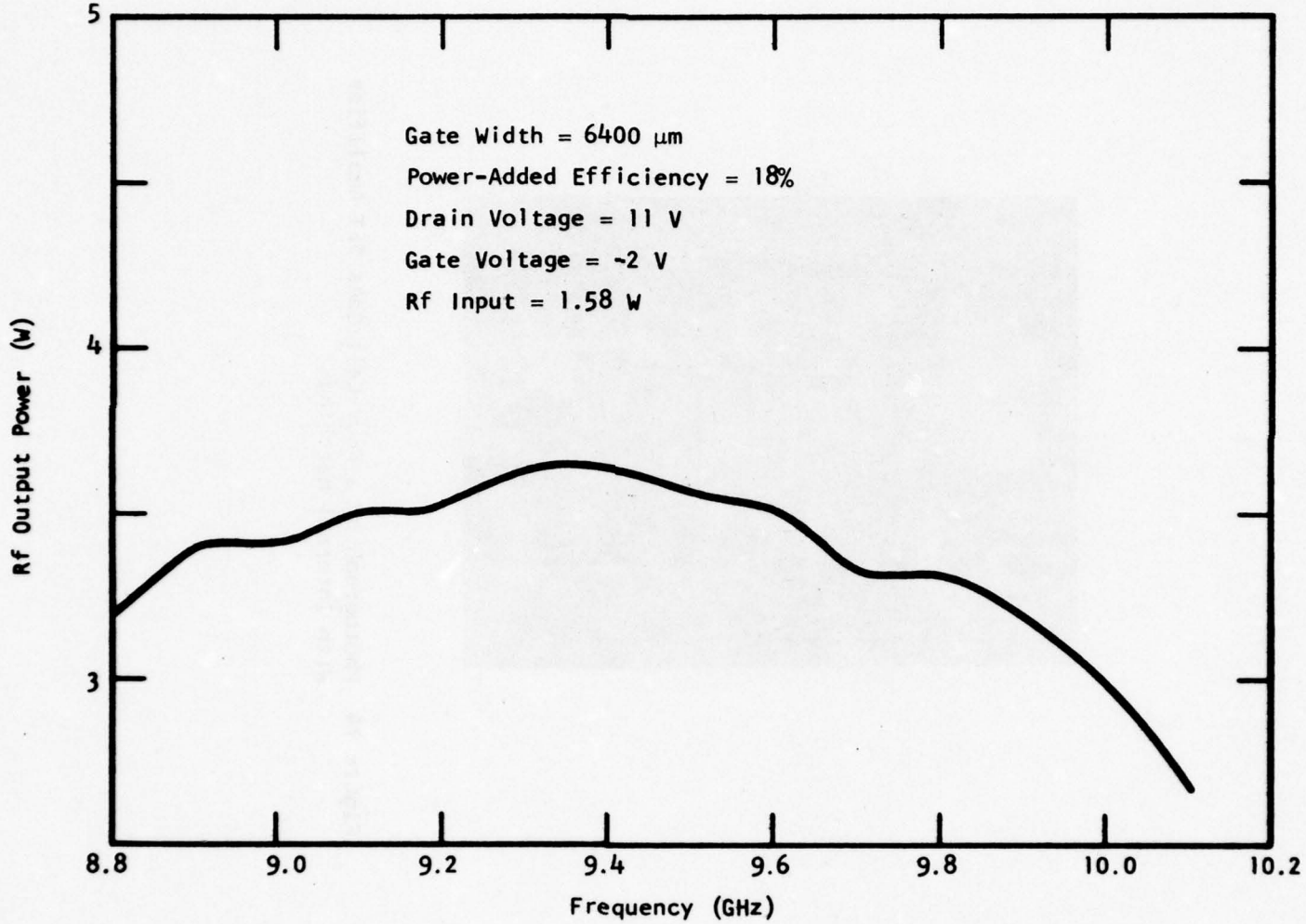


Figure 15 Output Power Frequency Response of a High-Power GaAs FET Amplifier

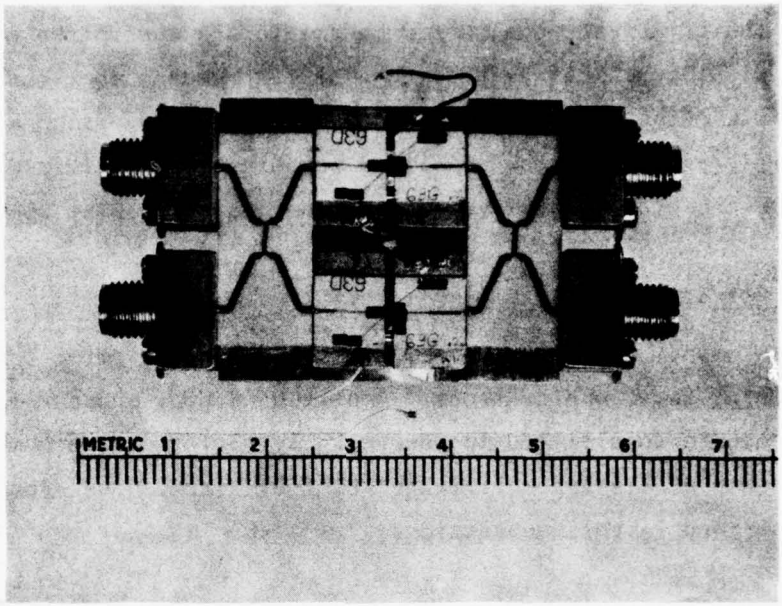


Figure 16 Test Fixture for a Single-Stage Balanced Amplifier

is shown in Figure 17. At 9.2 GHz, 5 W of output power with 25 dB gain can be obtained. The 1 dB bandwidth is 300 MHz (9.1 to 9.4 GHz). The efficiency is ~ 10%. The low efficiency and narrow bandwidth are due to the nonoptimum Read diode output stage. This Read diode amplifier uses a four-mesa diode and is capable of 10 W output at 4 dB gain with a dc-to-rf conversion efficiency of ~ 20%. As the diode size and the amplifier bandwidth are optimized, the hybrid amplifier can be expected to achieve the program goal of 5 W at 25 dB gain.

D. Pulsed Rf Characterization of Amplifiers

Pulse measurements were made on FET amplifiers to determine their suitability in phased-array radar applications. Amplitude droop, phase ramp, AM-to-PM conversion, and phase sensitivity to power supply variations were measured extensively on both single and multistage FET amplifiers. The measurement results are described in this subsection.

Figure 18 shows a block diagram of the basic measuring system suitable for pulsed and cw operation. A sweep oscillator capable of operating over the frequency band from 8 to 12 GHz provides frequency control of the test signal. A PIN diode modulator in conjunction with the master pulse generator establishes a pulsed rf signal of controlled duration and repetition rate. For cw measurements the PIN modulator is simply switched to the transmission mode. The signal from the output of the PIN modulator is then increased in magnitude by a TWT amplifier and monitored by power meter A. A level control signal is supplied by power meter A to the power meter level input on the sweep oscillator to ensure that the test signal input to precision attenuator A is of constant amplitude over the swept frequency band. The input power level to the amplifier under test is set by precision attenuator A. Power meter B is calibrated to read the output power of the test amplifier. The amplifier gain is determined from the readings of power meters A and B and precision attenuator A. An output signal from power meter B is supplied to the X-Y recorder, which records amplifier gain and output power as a function of

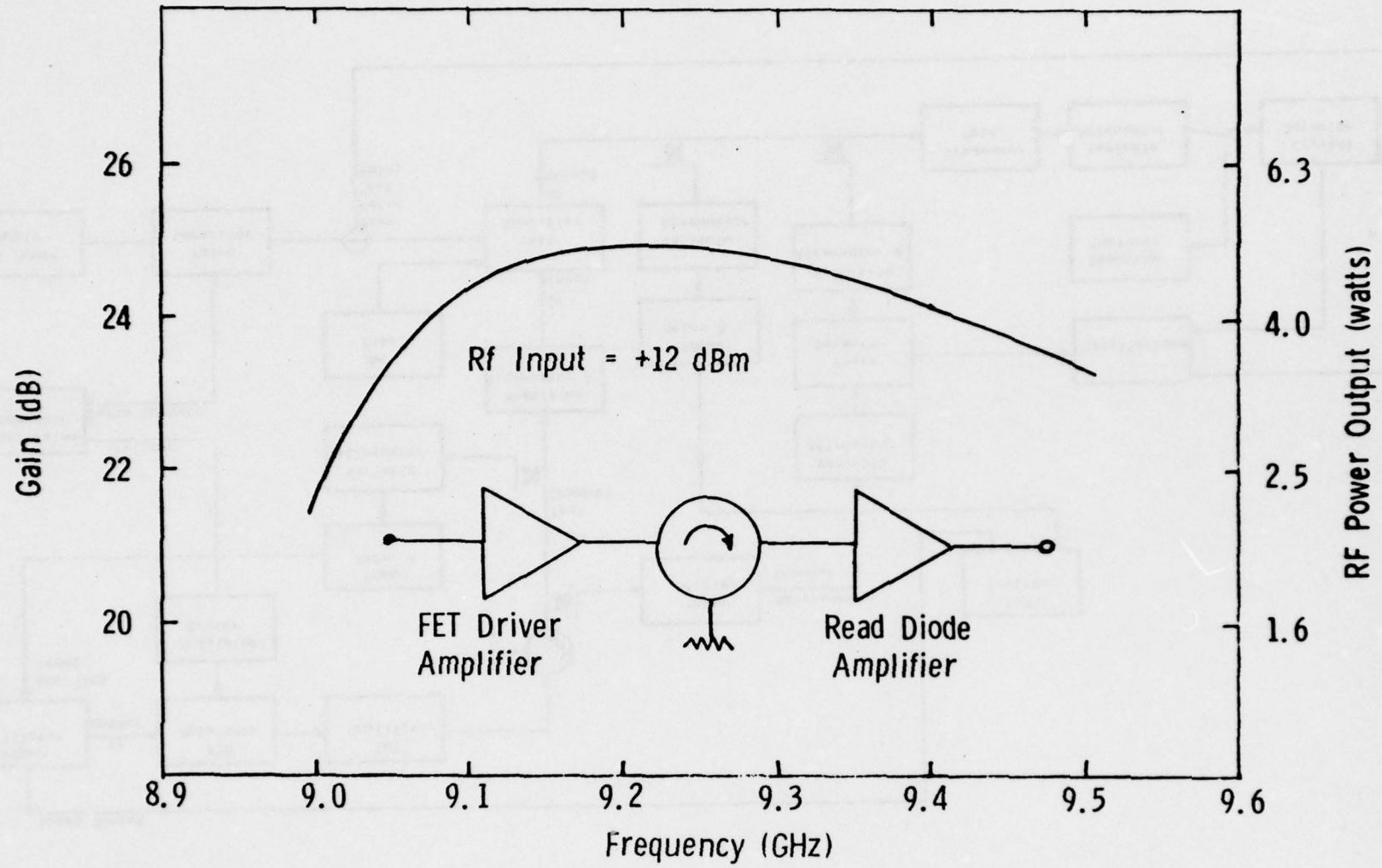


Figure 17 Microwave Performance of a Hybrid FET/Read Amplifier

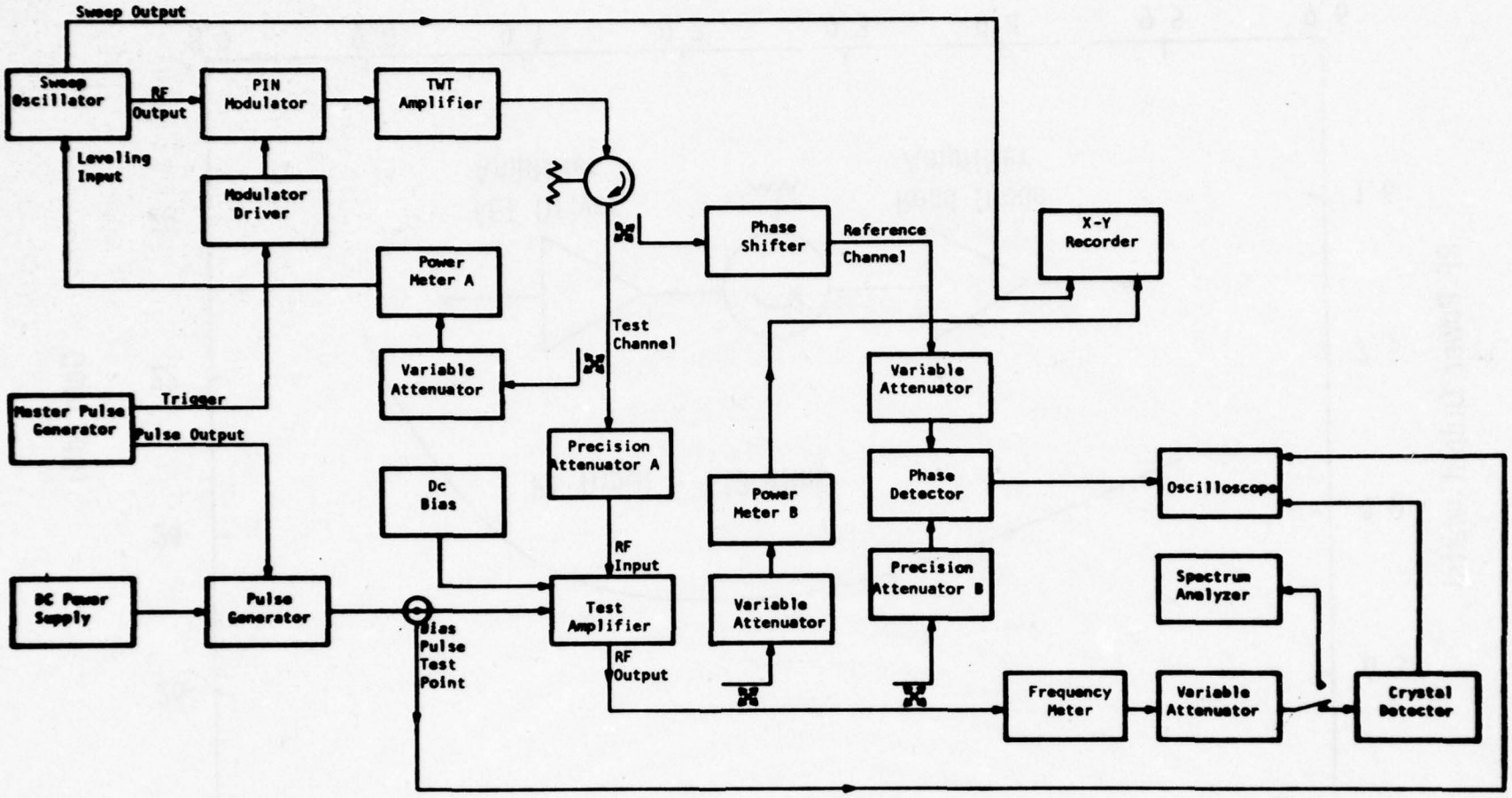


Figure 18 Block Diagram of Rf Test Setup for GaAs FET Amplifiers

frequency. Similarly, input VSWR as a function of frequency can be recorded by providing a directional coupler (not shown) between precision attenuator A and the amplifier input port and monitoring the reflected power with a power meter whose output can be fed to the X-Y recorder.

The amplifier output signal is coupled through a 10 dB coupler to precision attenuator B and then to the phase detector, completing the test channel leg of the phase bridge. The amplifier output is also supplied to a frequency meter and crystal detector. The crystal detector output is displayed on an oscilloscope for determination of the rf pulse characteristics. Rise and fall times, pulse amplitude droop, and intrapulse phase shift versus time are all measured from the detector output displayed on the oscilloscope. The crystal detector can be replaced with a spectrum analyzer for the measurement of spurious signals generated by the amplifier. The reference channel of the phase bridge is made up of a precision phase shifter, a level set attenuator, and a length of transmission line. The transmission line is used to equalize the time delay of the two channels. The precision phase shifter is used to null the phase bridge under varying test conditions and hence provides the relative phase data for phase response characterization. With the system in either cw or pulsed mode the phase bridge can be used to measure the AM-to-PM conversion. The input power to the amplifier is adjusted with precision attenuator A, while any change of phase shift through the amplifier is detected on the phase bridge.

1. Amplitude Droop

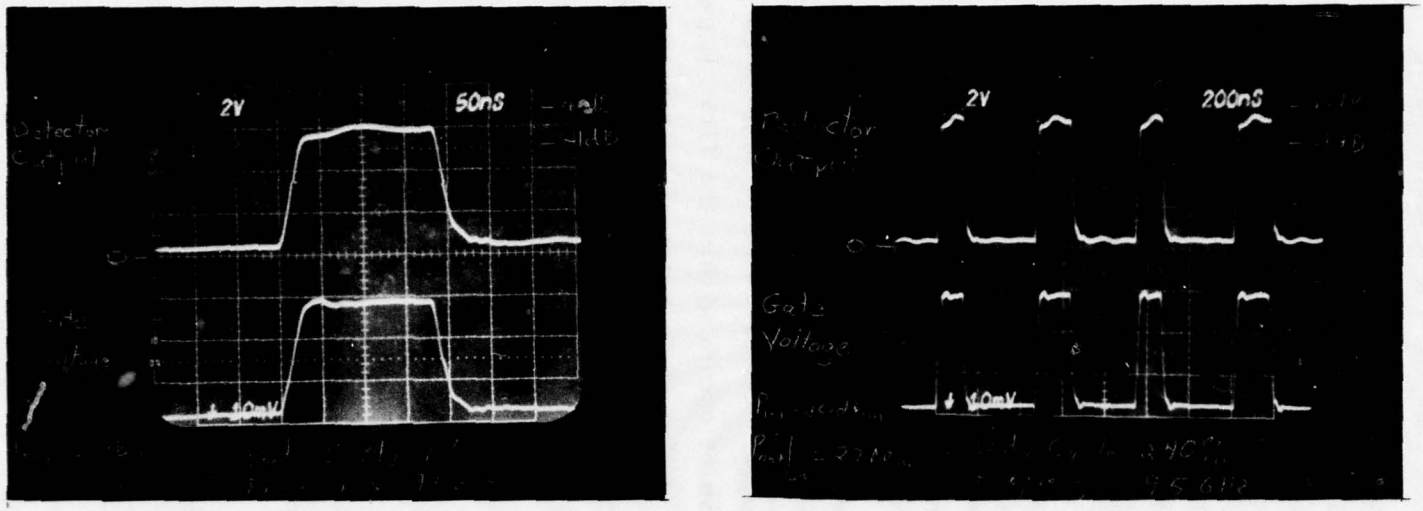
The amplitude droop in most cases remains less than 0.5 dB for pulse widths up to 50 μs. The gate voltage of the FET is pulsed from the pinch-off to the nominal gate bias. The input rf can be either a cw signal or a pulsed signal in synchronization with the gate bias pulse. The drain voltage is maintained at a constant value. Single-cell and multicell FETs (up to a total gate width of 3600 μm) have been evaluated under pulse conditions.

A three-stage, 0.5 W FET amplifier was also pulse-operated with pulse widths ranging from 200 ns to 20 μs and duty cycles of less than 1% to 40%. A risetime of 30 ns was achieved for the output rf pulse. Total variation of output power within the pulse was less than 0.75 dB for the range of pulse widths and duty cycles specified above. Figures 19(a) and 19(b) show the detected rf power output and gate voltage waveforms, as traced on an oscilloscope, for 1% and 40% duty cycle operation, respectively. The second horizontal graticule line from the top is the cw reference power level and corresponds to 30 dBm. For pulse operation the gate voltage was biased from a value near that corresponding to pinch-off (-7.5 V) to the nominal cw value corresponding to 0.5 W output power.

In the bias circuit design of FET amplifiers it is often necessary to use a shunt capacitor ($\sim$ 0.01 μF) across the gate bias choke to prevent build-up of low-frequency oscillation. Although this scheme is satisfactory for cw operation of the FET amplifier, it is not suitable for pulse operation, since it degrades the rise/fall time of the gate bias pulse. To overcome this problem, a chip resistor (50 $\sim$ 100 Ω) can be used in series with the bias circuit for stability and fast response time of the FET amplifiers. To be effective, this resistor should be connected as closely as possible to the device.

2. Phase Ramp

The intrapulse phase shift was measured to be less than 2° for single-stage amplifiers and for maximum pulse width up to 50 μs. The pulse scheme is such that the turn-on gate pulse (the FETs were biased at pinch-off for standby) can be advanced or delayed with respect to the input rf pulse. It is observed that, to minimize the phase spike during the turn-on transient (of 30 to 40 ns duration), the gate turn-on pulse needs to be advanced. This minimizes the phase transient due to the changing gate voltage during the turn-on, since it is found that the insertion phase is a sensitive function of the gate voltage.



Duty Cycle 1%

(a)

Duty Cycle ≈ 40%

(b)

3-Stage FET Amplifier

P_{in} = 10 dBm, $P_{out}\Big|_{cw}$ = 27 dBm

Frequency: 9.5 GHz

V_D = 9.5, I_D = 560 mA, V_G = -2.2

η_{cw} = 10%

Figure 19 Detected rf Power Output and Gate Voltage for (a) 1% Duty Cycle and (b) 40% Duty Cycle Operation

Figure 20 illustrates the effects of changing the relative pulse widths of the rf and gate pulses on the phase transient for a 300 μm gate width FET at 9.5 GHz. From these figures, it is clear that, to minimize the phase transient during the rise and fall times of the gate pulse, the gate pulse width needs to be wider than the rf pulse width. Figure 21 shows the intrapulse phase shift of the same amplifier at a pulse width of 50 μs and at two duty factors (2.85% and 25%). A maximum phase shift of 1.5° was observed. It should be noted that the phase bridge was adjusted for a null at the leading edge of the phase ramp.

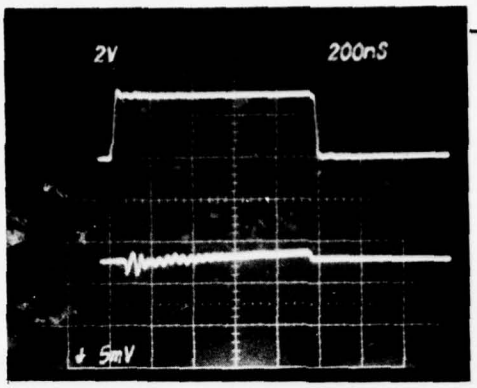
Figure 22 shows the intrapulse phase shift of a 1200 μm gate width FET amplifier at three input power levels and two different pulse widths (200 μs and 50 μs). The phase response of a 3600 μm gate width FET is shown in Figure 23. For a 10 μs pulse width a maximum phase shift of less than 2° is observed. The result of preliminary phase ramp measurement on a three-stage, 0.5 W amplifier is shown in Figure 24. A phase shift of 8° for a 50 μs pulse width is seen. However, most of the phase shift occurs within the first 10 μs. Additional data will be gathered on the intrapulse phase shift of multistage amplifiers during the next report period. Since the intrapulse phase shift is of thermal origin, it is conceivable that, with a proper thermal design, this shift can be minimized.

3. AM-to-PM Conversion

The AM-to-PM conversion remains below 3°/dB for input drive levels up to the 1 dB gain compression point. The AM-to-PM conversion is independent of the operation modes, i.e., either cw or pulsed. Figure 25 shows the AM-to-PM conversion characteristic of a single-stage and a three-stage amplifier. The phase shift is taken as zero at the nominal rf input level of the amplifiers.

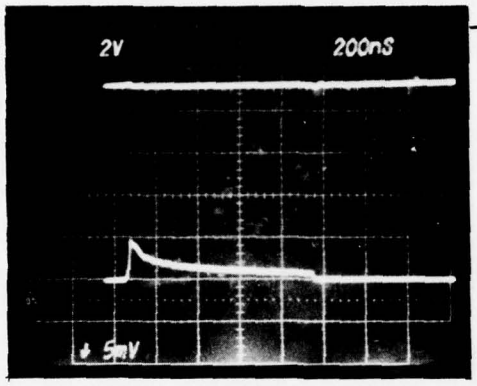
4. Phase Sensitivity to Power Supply Variations

The insertion phase is far more sensitive to the gate voltage variation then to the drain voltage variations. Figure 26 shows the bias

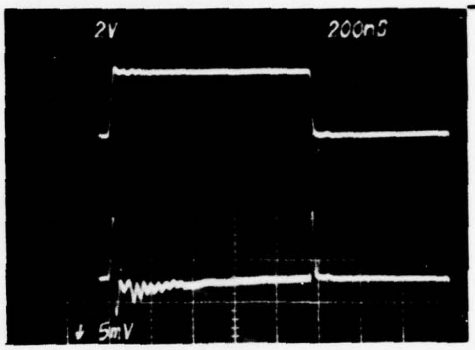


(a)

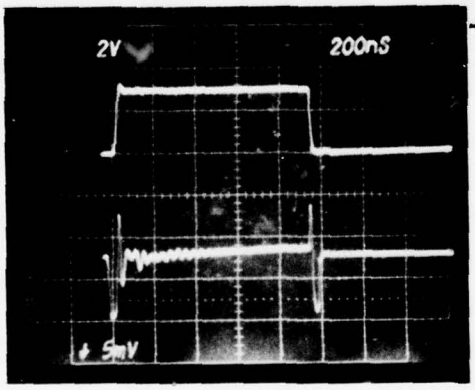
Frequency = 9.5 GHz
P_{in} = 10 dBm
V_{gs} = -6 V OFF
-3 V ON
V_{ds} = 6 V
Pulse Width = 1 μs
Duty Cycle = 5%



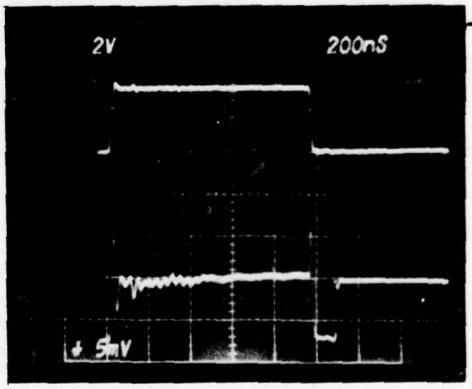
(b)



(c)



(d)



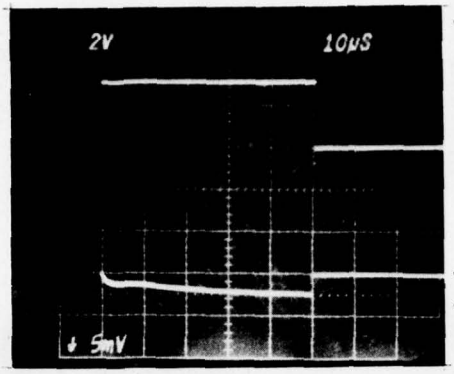
(e)

Figure 20 Pulsed Phase Response of a 300 μm Gate Width FET Amplifier Under Various Operating Conditions. Upper Trace: Gate Voltage; Lower Trace: Phase Shift. (a) Gate Voltage pulse width > rf pulse width; (b) rf pulsed with cw gate bias; (c) gate voltage pulsed with cw rf; (d) gate voltage pulse width = rf pulse width; (e) gate voltage pulse width < rf pulse width

Frequency = 9.5 GHz

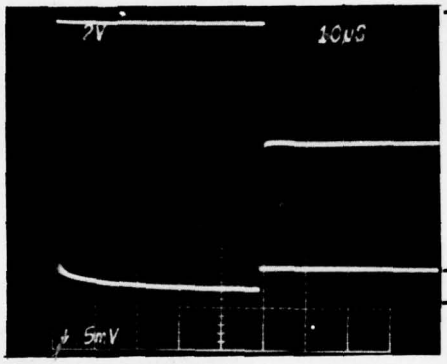
P_{in} = 10 dBm
P_{out} = 20 dBm

V_{ds} = 6 V
V_{gs} = -6 V off
-3 V on



—-0 V
Gate Voltage
$\Delta\phi$ = 1.5°

Pulse Width = 50 μs
Duty Dycle = 25%

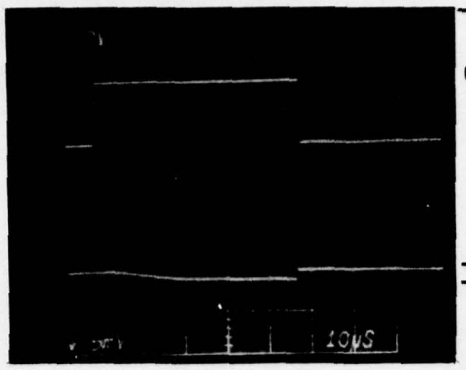


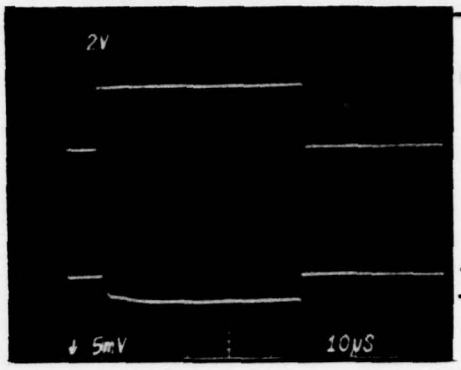
—-0 V
Gate Voltage
$\Delta\phi$ = 1°

Pulse Width = 50 μs
Duty Cycle = 2.85%

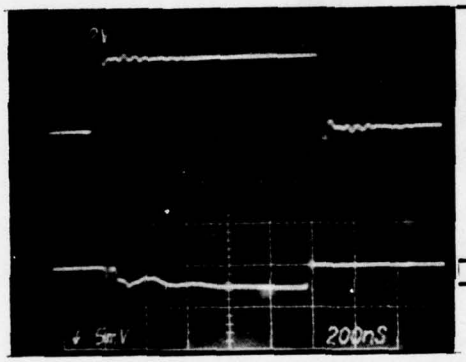
Figure 21 Intrapulse Phase Shift of a 300 μm Gate Width FET Amplifier With 50 μs Pulse Width

V_{gs} = -6 V off
-3 V on

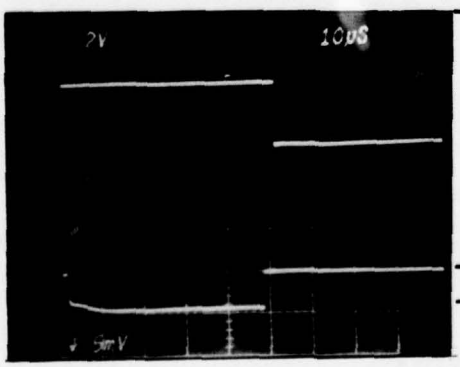




Pin = 15 dBm Pulse Width = 50 μs Pin = 20 dBm
Duty Cycle = 25%



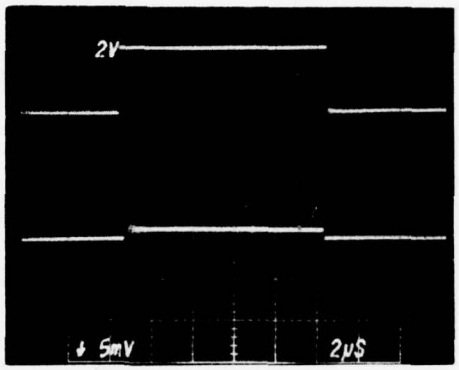
Pulse Width = 1 μ
Duty Cycle = 1%
Pin = 20 dBm



Pulse Width = 50 μs
Duty Cycle = 25%

Pin = 23 dBm

Figure 22 Intrapulse Phase Shift of a 1200 μm Gate Width FET at Different Rf Input Levels and Pulse Widths



— -0

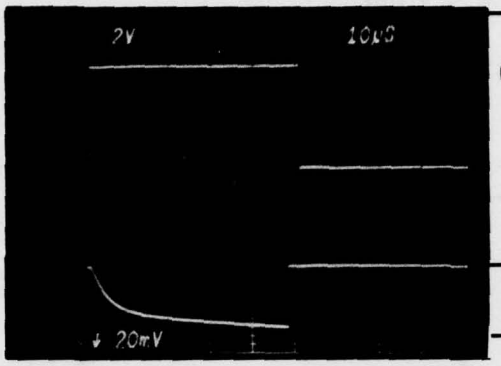
Gate Voltage

2°/div

Frequency = 9.5 GHz
Gate Width = 3600 µm
V_{ds} = 7 V
Rf Input = 23 dBm
Gain = 5 dB
Pulse Width = 10 µs
Duty Cycle = 1%

Figure 23 Pulsed Phase Response of a 3600 µm Gate Width FET

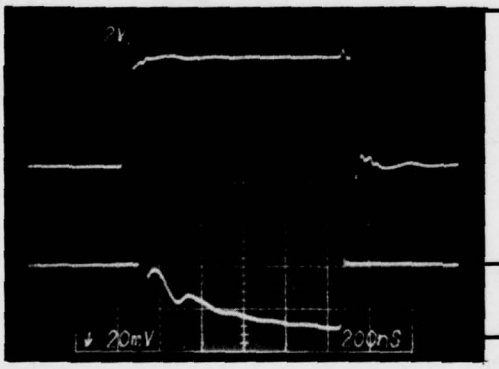
Frequency = 9.5 GHz P_{in} = 10 dBm P_{out} = 27 dBm V_{gs} = -7 V off, -2.5 V on



-0

Gate Voltage

$\Delta\phi$ = 8°



-0 V

Pulse Width = 1 μs
Duty Cycle = ½%

$\Delta\phi$ = 7°

Figure 24 Pulsed Phase Response of a Three-Stage GaAs FET Amplifier at Pulse Widths of 1 μs and 50 μs

Pulse Width = 50 μs
Duty Cycle = 25%
Frequency = 9.5 GHz

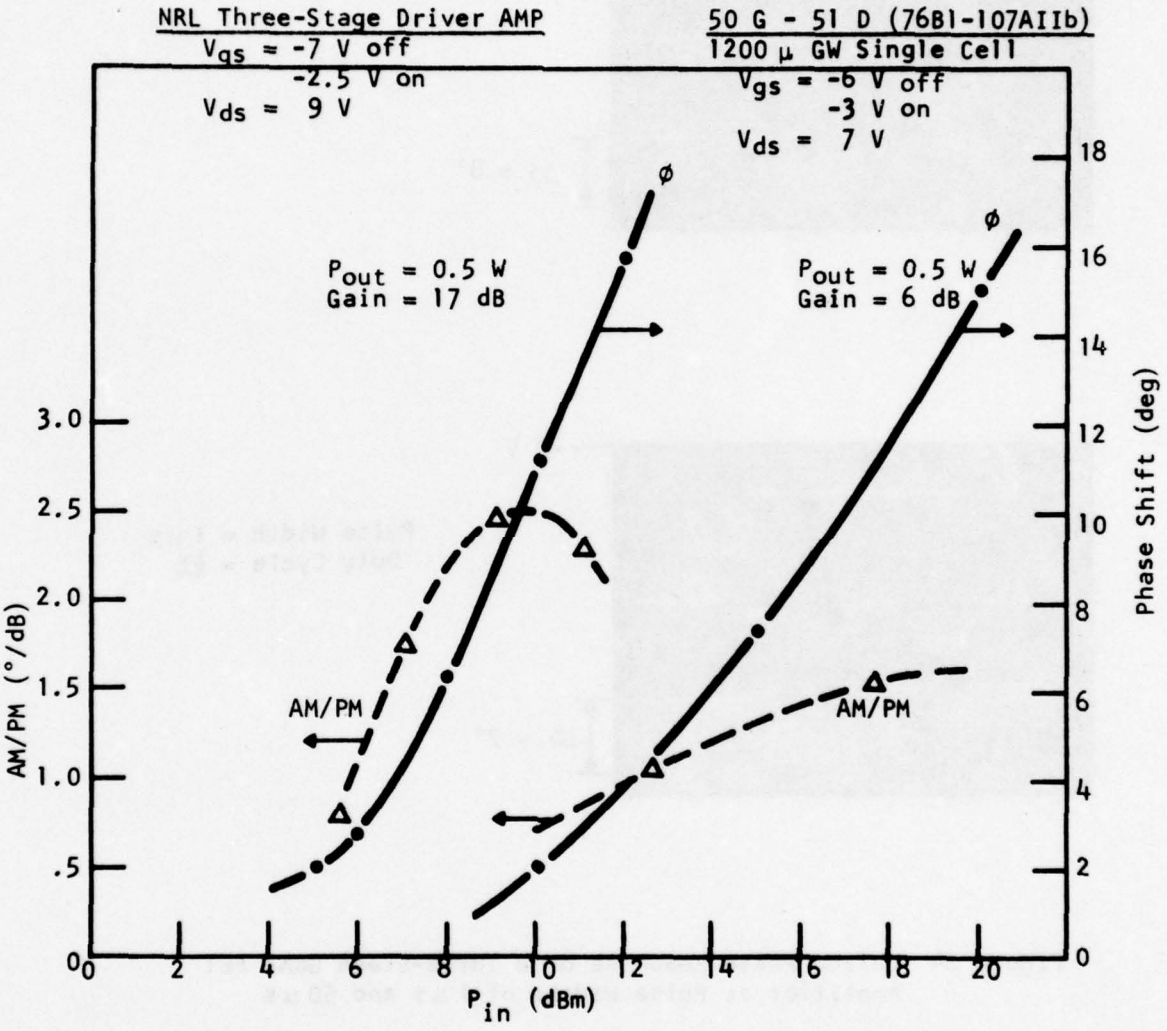


Figure 25 AM to PM Conversion Characteristics of a Single-Stage and a Three-Stage GaAs FET Amplifier

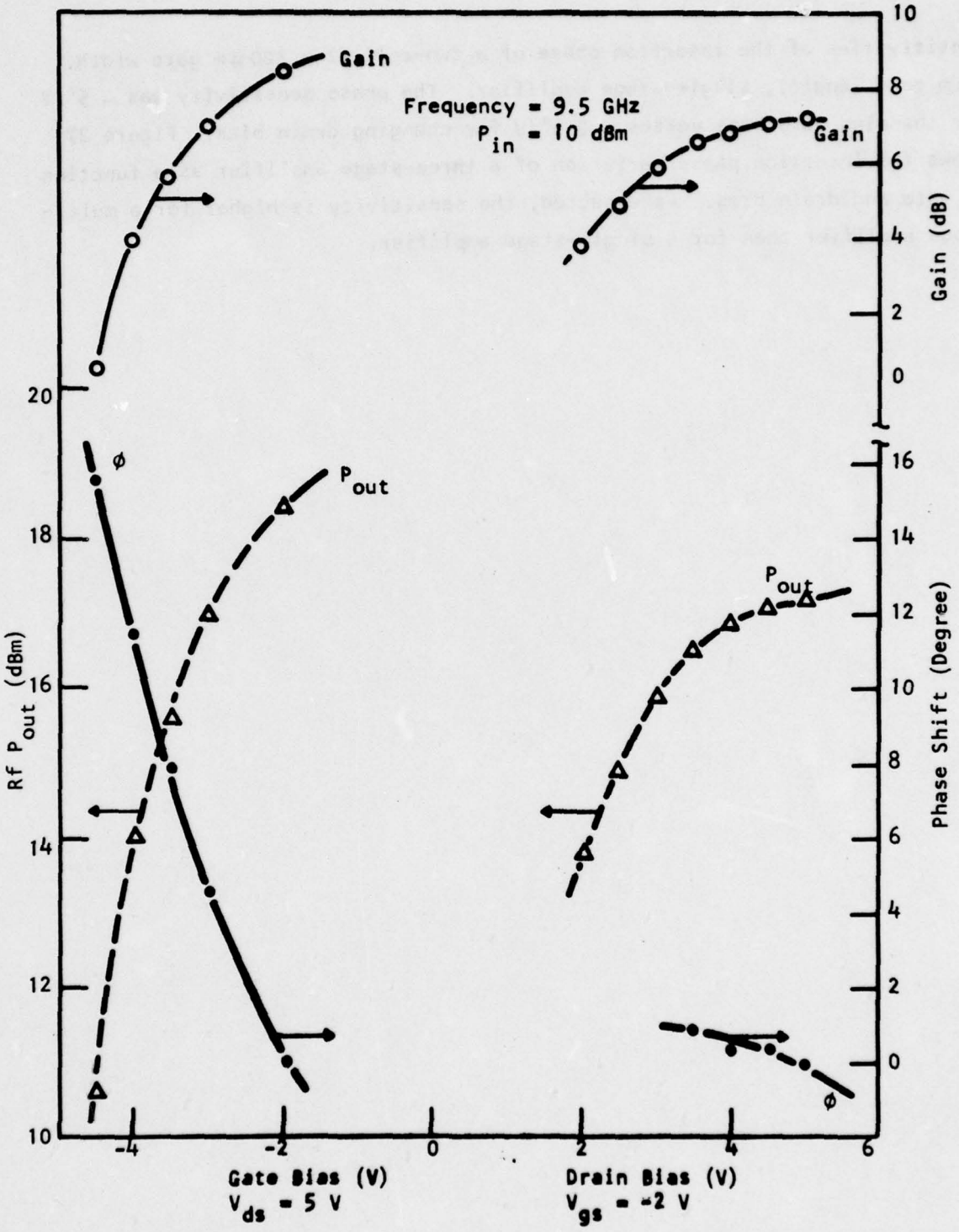


Figure 26 Bias Sensitivity of the Insertion Phase of a 600 μm Gate Width GaAs FET Amplifier

sensitivities of the insertion phase of a two-cell (2 x 300 μm gate width, 1 μm gate length), single-stage amplifier. The phase sensitivity was ~ 5°/V for changing gate bias versus ~ 0.3°/V for changing drain bias. Figure 27 shows the insertion phase variation of a three-stage amplifier as a function of gate and drain bias. As expected, the sensitivity is higher for a multi-stage amplifier than for a single-stage amplifier.

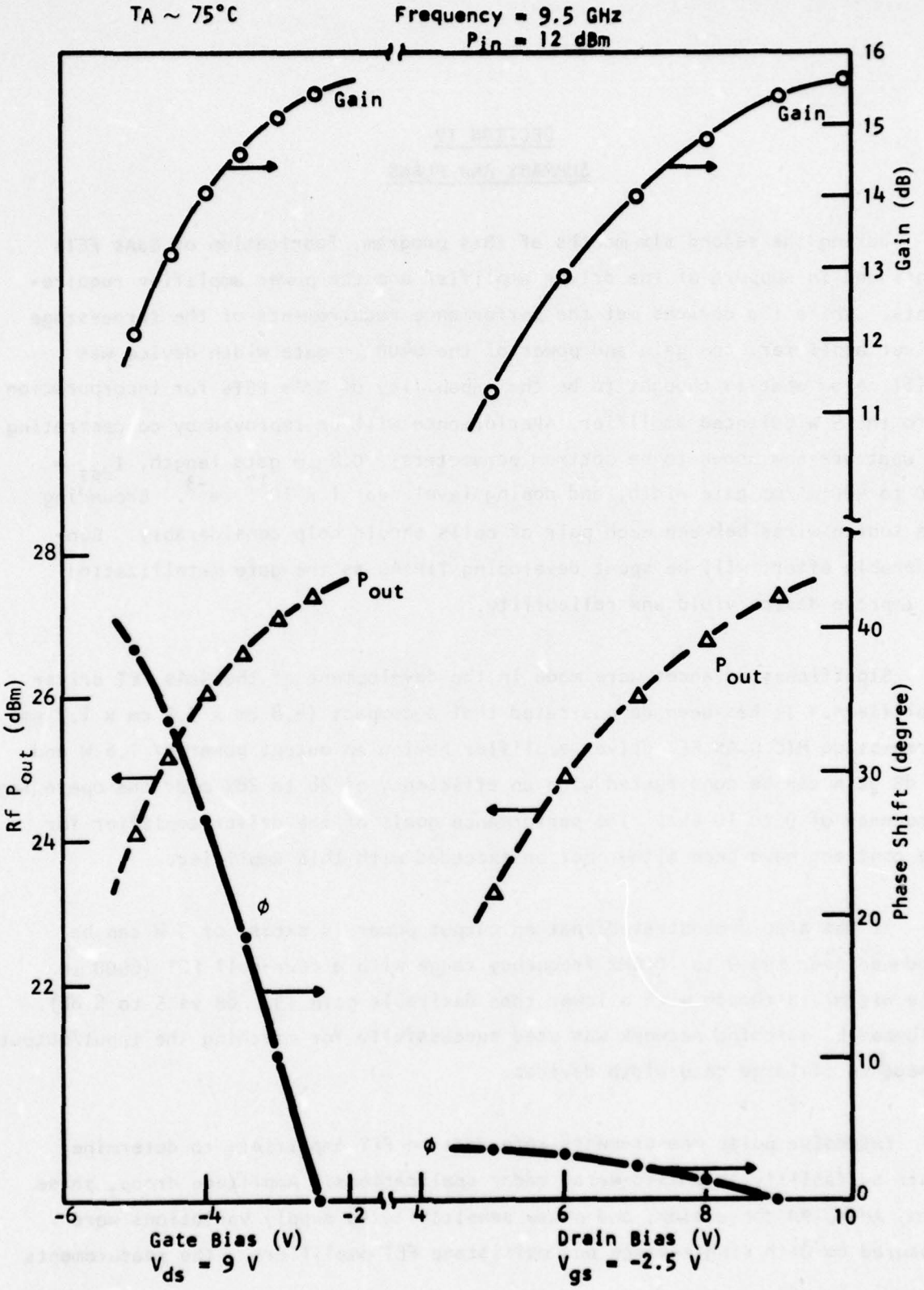


Figure 27 Insertion Phase as Function of Bias Voltages for a Three-Stage GaAs FET Amplifiers

SECTION IV
SUMMARY AND PLANS

During the second six months of this program, fabrication of GaAs FETs continued in support of the driver amplifier and the power amplifier requirements. While the devices met the performance requirements of the three-stage driver amplifier, the gain and power of the 6400 μm gate width device was still below what is thought to be the capability of GaAs FETs for incorporation into the 5 W balanced amplifier. Performance will be improved by concentrating on what are now known to be optimum parameters: 0.8 μm gate length, I_{dss} = 330 to 400 mA/mm gate width, and doping level near 1×10^{17} cm^{-3}. Grounding the source wires between each pair of cells should help considerably. Considerable effort will be spent developing TiPtAu as the gate metallization to improve device yield and reliability.

Significant advances were made in the development of the GaAs FET driver amplifiers. It has been demonstrated that a compact (4.8 cm x 3.3 cm x 1.7 cm) three-stage MIC GaAs FET driver amplifier having an output power of 1.6 W and 20 dB gain can be constructed with an efficiency of 26 to 28% over the operating frequency of 9 to 10 GHz. The performance goals of the driver amplifier for the contract have been either met or exceeded with this amplifier.

It was also demonstrated that an output power in excess of 3 W can be produced over the 9 to 10 GHz frequency range with a four-cell FET (6400 μm gate width), although with a lower than desirable gain (3.6 dB vs 5 to 6 dB). A lumped LC matching network was used successfully for matching the input/output impedance of large gate width devices.

Extensive pulse measurements were made on FET amplifiers to determine their suitability in phased-array radar applications. Amplitude droop, phase ramp, AM-to-PM conversion, and phase sensitivity to supply variations were measured on both single-stage and multistage FET amplifiers. The measurements

indicate that there is no significant limitation in using power GaAs FETs in active-element, phased-array radar systems.

In addition to improving the yield and gain of the 6400 μm FET for the remaining six-month period of the contract, the major effort planned in the circuit area will be to develop the 5 W, 5 dB gain FET and Read diode power amplifiers. Particular emphasis will be placed on the combining efficiency of the 5 W balanced FET amplifier stage. The 5 W, 25 dB gain solid-state module will then be developed by cascading the driver amplifier with either the 5 W FET or the Read diode amplifier stage. Rf characterization will be extensively performed on the modules to be delivered to NRL at the end of the contract.

APPENDIX

DEVICE DELIVERIES

Table A1

Devices Delivered to NRL - May 1977

GaAs FET Microwave Performance at 10 GHz

Number	Slice Identification	Good Cells	V_p (V)	Gain (dB) P_{in} = 15 dBm V_{ds} = 5V $V_g \cong 0$	Maximum P_{out} (W) with 4dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (V)	Maximum P_{out} (W) with 6dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (v)	Maximum P_{out} (W) with 4 dB Gain V_{ds} = 10V
1	76B1-108B1e	1,2	5.5	6.9	1.51	28	405	-2.9	-	-	-	-	1.86
2	76B1-108B1e	1,2	8.2	6.4	1.38	20	530	-3.0	-	-	-	-	1.44
3	76B1-108B1e	3	6.1	7.6	1.09	36	230	-2.6	0.76	30	235	-2.6	1.26
4	76B1-108B1e	2	9.1	7.0	0.78	30	190	-3.1	0.48	23	190	-3.4	0.89
5	76B1-137B1e	1,2	4.5	6.5	1.44	29	375	-1.6	-	-	-	-	1.86
6	77B1-2B1e	1	3.4	7.5	0.95	40	180	-1.0	0.76	36	190	-1.1	1.20
7	77B1-2B1e	3,4	3.5	7.7	1.58	36	335	-1.6	1.20	28.5	395	-1.3	1.99
8	77B1-2B1e	1	3.5	7.2	0.95	37	190	-1.75	0.69	29	225	-1	1.17
9	76B1-137B1e	4	3.4	7.2	0.91	39	175	-1.2	0.72	35	190	-1	1.07
10	76B1-137B1e	2	3.9	7.0	0.89	36	185	-1.6	0.63	29	200	-1.5	1.12

Table A2

GaAs Read Diodes Delivered to NRL - May 1977

Diode No.	V_B (V)	V_{op} (V)	I_{op} (mA)	Prf (W)	η (%)	f (GHz)
C27B	6013	59.1	267	3.4	17.2	9.05
C87B	6022	57.1	355	5.0	24.7	8.4
C89B	6026	51.5	471	4.6	19.0	8.5
C89B	6027	54.0	443	4.5	18.8	8.5
C51B	6030	52.7	442	4.0	17.2	9.2
C51B	6037	56.9	392	3.7	16.6	8.8
C21B	6039	56.9	313	3.4	18.4	8.6
C21B	6040	60.7	364	3.8	17.2	8.6
C21B	6047	56.6	386	3.7	16.9	8.8
C122	6043	55.8	275	3.6	23.5	9.6

Table A3

Devices Delivered to NRL - July 1977

GaAs FET Microwave Performance at 10 GHz

Number (Slice 76B1-91A IIe)	Good Cells	V_p (V)	Gain (dB) P_{in} = 15 dBm V_{ds} = 5V V_g = -1V	Max P_{out}(W) w/4 dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (V)	Max P_{out}(W) w/4 dB Gain V_{ds} = 10V	Max P_{out}(W) w/6 dB Gain V_{ds} = 8V	Power-Added Eff. (%)	I_{ds} (mA)	V_g (V)
1	3,4	5.8	6.6	1.66	31	408	-1.9	2.09	0.91	15	582	-1.1
2*	2,3,4	5.6	7.5	2.40	31	587	-2	2.82	1.44	22	615	-2
3	1,2	5.1	6.4	1.51	32	361	-1.7	1.82	-	-	-	-
4	2	5.7	7.2	1.10	32	255	-2	1.20	0.79	31	240	-2.5
5	1	4.5	6.7	0.83	33	187	-1.4	1.02	0.56	21	248	-1.1
6	2,3	6.5	6.4	1.66	35	356	-2.9	1.95	-	-	-	-
7*	2,3,4	5.6	6.0	2.19	35	471	-2.6	2.51	-	-	-	-
8	2,3	3.8	6.6	1.41	33	323	-1	1.91	1.02	24	405	-0.8
9	1,2	6.7	6.1	1.62	30	404	-2.6	2.19	-	-	-	-
10	2,3	6.0	6.3	1.38	31	337	-2.4	1.70	-	-	-	-

*Data taken at 8 GHz.

H. M. Macksey
July 20, 1977

Table A4

GaAs Read Diodes Delivered to NRL - July 1977

Diode No.	V_B (V)	V_{op} (V)	I_{op} (mA)	P_o (W)	P_{rf} (W)	η (%)	f (GHz)
6038	35.8	54.6	463	25.2	4.84	19.1	8.8
6048	37.2	54.6	443	24.1	5.05	21.0	9.4
6052	37.4	53.1	480	25.4	5.63	22.0	9.2
6054	39.5	56.8	356	20.2	4.5	22.2	9.3
6057	39.6	58.6	339	19.8	4.3	21.6	9.0
6058	40.2	57.7	370	21.3	4.63	21.6	9.4
6058.1	39.4	57.5	368	21.1	4.53	21.6	9.4
6061	38.6	57.9	373	21.6	4.6	21.2	9.3
6063	38.3	56.8	381	21.6	5.0	23.1	8.7
6064	38.0	57.7	392	22.6	5.0	22.0	9.6

Table A5

Devices Delivered to NRL - September 1977

Device Number	Slice Number	Good Cells	V_p (V)	Frequency (GHz)	Gain (dB) P_{in} = 15 dB V_{ds} = 5V V_g = -1V	Max P_{out} (W) with 4 dB Gain V_{ds} = 8V	Power-Added Efficiency (%)	I_{ds} (mA)	V_g (V)	Max P_{out} (W) with 4 dB Gain V_{ds} = 10V	Max P_{out} (W) with 6 dB Gain V_{ds} = 8V	Power-Added Efficiency (%)	I_{ds} (mA)	V_g (V)
1	76B1-91AIIe	1,2,3,4	5.3	8	6.6	2.57	29.3	660	-2.75	3.16	1.20	10.5	1070	-1.0
2	76B1-91AIIe	1,2,3,4	6.2	8	6.8	3.80	30.5	935	-2.1	4.36	1.90	15.3	1160	-1.7
3	76B1-91AIIe	1,2,3,4	5.1	8	6.5	2.51	29.4	640	-2.45	-	1.25	11.2	1050	-1.1
4	77B1-85BIe	1,2,3,4	5.6	8	8.9	3.16	33.2	715	-1.95	4.07	2.34	25.1	870	-1.9
5	77B1-85BIe	1,2,3,4	5.4	8	8.8	2.88	29.5	735	-2.15	3.63	2.09	23.6	830	-1.9
6	77B1-81BIe	1	4.5	10	6.8	0.72	36.0	150	-1.5	0.91	0.50	27.3	170	-1.5
7	77B1-81BIe	1	4.9	10	6.8	0.85	35.6	180	-1.25	1.05	0.56	24.9	210	-1.25
8	77B1-81BIe	1	4.9	10	6.8	0.87	36.0	180	-1.0	1.12	0.62	28.4	200	-1.0
9	77B1-81BIe	1	3.9	10	7.4	0.95	37.6	190	-1.0	1.15	0.72	33.4	200	-0.8
10	77B1-22BIe	1	~9.0	10	7.0	0.69	29.9	175	-2.8	0.81	0.40	15.4	240	-1.8

Table A6

GaAs Read Diodes Delivered to NRL - September 1977

Diode No.	V_B (V)	V_{op} (V)	I_{op} (mA)	P_o (W)	P_{rf} (W)	η (%)	f (GHz)
6056	38.8	55.9	416	23.2	5.32	22.8	9.2
6062	38.9	56.2	393	22.0	5.2	23.5	9.3
6055	40.0	57.0	401	22.8	5.0	21.8	9.3
6059	38.2	56.3	397	22.4	5.25	23.5	9.3
6060	38.4	56.7	402	22.8	5.72	25.0	9.3
6049	41.9	52.5	467	24.5	5.15	21.0	9.2
6050	35.9	52	475	24.7	5.9	23.8	9.2
6066	40.1	58.4	416	24.2	5.0	20.5	8.7
6065	40.7	58.7	447	26.2	6.06	23.0	8.9
6067	38.4	57.2	485	27.7	5.8	20.8	8.9

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